SEMICONDUCTOR DATA BOOK
HITACHI IC MEMORIES

HITACHI

INDEX

NOTICE

The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of a semiconductor-applied products. The Company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

CURRENT LINE OF HITACHI IC MEMORIES

● MOS Memory

- MOS Memory
  - RAM
    - Dynamic
      - NMOS
        - 16k-bit
          - 16384×1
            - 3 Supplies: HM4716A-1 — HM4716A-2 — HM4716A-3 — HM4716A-4
            - Single Supply: HM4816A-3 — HM4816A-4 — HM4816A-7
        - 64k-bit
          - 65536×1: HM4864-2 — HM4864-3 — HM4864A-12* — HM4864A-15* — HM4864A-20*
    - Static
      - NMOS
        - 4k-bit
          - 1024×4: HM472114A-1 — HM472114A-2 — HM472114-3 — HM472114-4
      - CMOS
        - 4k-bit
          - 4096×1: HM4315 — HM6147/L — HM6147/L-3 — HM6147H/L-35* — HM6147H/L-45*
          - 1024×4: HM4334/L-3 — HM4334/L-4 — HM6148/L — HM6148 L-6
      - CMOS
        - 16k-bit
          - 16384×1: HM6167/L — HM6167/L-6 — HM6167/L-8
          - 2048×8: HM6116/L-2 — HM6116/L-3 — HM6116/L-4 — HM6117/L-3* — HM6117/L-4*
  - ROM
    - Mask ROM
      - NMOS
        - 32k-bit
          - 4096×8: HN46332
        - 64k-bit
          - 8192×8: HN48364
      - CMOS
        - 128k-bit
          - 16384×8 or 32768×4: HN43128
          - 16384×8: HN613128*
        - 256k-bit
          - 32768×8 or 65536×4: HN61256
    - EP ROM
      - NMOS
        - 16k-bit
          - 2048×8: HN462716 — HN462716-1 — HN462716-2
        - 32k-bit
          - 4096×8: HN462532 — HN462532-2 — HN462532L — HN462732 — HN462732-2 — HN482732A**
        - 64k-bit
          - 8192×8: HN482764* — HN482764-3* — HN482764-4
    - EEP ROM
      - NMOS
        - 16k-bit
          - 2048×8: HN48016*

* Preliminary
** Under development

● Bipolar Memory

- RAM
  - ECL 10k
    - 256-bit
      - 256×1: HM2105 — HM2106 — HM10414 — HM10414-1
    - 1k-bit
      - 1024×1: HM2110 — HM2110-1 — HM2110-2 — HM2112 — HM2112-1
      - 256×4: HM10422
    - 4k-bit
      - 4096×1: HM10470 — HM10470-1
      - 1024×4: HM10474
  - ECL 100k
    - 1k-bit
      - 1024×1: HM100415*
      - 256×4: HM100422
    - 4k-bit
      - 4096×1: HM100470
      - 1024×4: HM100474
  - TTL
    - 256-bit
      - 256×1
        - O/C: HM2504 — HM2504-1
    - 1k-bit
      - 1024×1
        - O/C: HM2510 — HM2510-1 — HM2510-2
        - 3-S: HM2511 — HM2511-1
- P ROM
  - TTL
    - 4k-bit
      - 1024×4
        - O/C: HN25044
        - 3-S: HN25045
    - 8k-bit
      - 2048×4
        - O/C: HN25084/S
        - 3-S: HN25085/S
      - 1024×8
        - O/C: HN25088/S
        - 3-S: HN25089/S
    - 16k-bit
      - 2048×8
        - O/C: HN25168S*
        - 3-S: HN25169S*

* Preliminary

TYPICAL CHARACTERISTICS OF MOS MEMORY

● MOS RAM

Mode	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns) max	Cycle Time (ns) min	Supply Voltage (V)	Power Dissipation (W)	Package** Pin No.	C	G	P	FP	Replacement	Page
Static	4k-bit	HM472114A-1	NMOS	1024×4	150	150	+5	0.2	18		●	●			46
		HM472114A-2			200	200					●	●		2114L-2	46
		HM472114-3			300	300					●	●		2114L-3	50
		HM472114-4			450	450					●	●		2114L-4	50
		HM4334-3	CMOS	1024×4	300	460	+5	10μ/20m	18		●	●		HM-6514	53
		HM4334-4			450	640					●	●			53
		HM4334-3L			300	460		10μ/20m				●			58
		HM4334-4L			450	640						●			58
		HM6148	CMOS	1024×4	70	70	+5	0.1m/0.2	18		●	●		2148	63
		HM6148-6			85	85					●	●		2148-6	63
		HM6148L			70	70		5μ/0.2				●			69
		HM6148L-6			85	85						●			69
		HM4315	CMOS	4096×1	450	640	+5	10μ/20m	18			●		HM-6504	75
		HM6147	CMOS	4096×1	70	70	+5	0.1m/75m	18		●	●		2147	80
		HM6147-3			55	55					●	●		2147-3	80
		HM6147L			70	70		5μ/5m				●			84
		HM6147L-3			55	55						●			84
		HM6147H-35*	CMOS	4096×1	35	35	+5	0.1m/0.15	18		●	●		2147H-1	88
		HM6147H-45*			45	45					●	●		2147H-2	88
		HM6147HL-35*			35	35		5μ/0.15				●			92
		HM6147HL-45*			45	45						●			92
	16k-bit	HM6116-2	CMOS	2048×8	120	120	+5	0.1m/0.18	24		●	●	●		96
		HM6116-3			150	150					●	●	●		96
		HM6116-4			200	200					●	●	●		96
		HM6116L-2			120	120		$20\overset{\triangle}{\mu}$/0.16			●	●	●		107
		HM6116L-3			150	150					●	●	●		107
		HM6116L-4			200	200					●	●	●		107
		HM6117-3*	CMOS	2048×8	150	150	+5	0.1m/0.2	24			●	●		125
		HM6117-4*			200	200						●	●		125
		HM6117L-3*			150	150		10μ/0.2				●	●		135
		HM6117L-4*			200	200						●	●		135
		HM6167	CMOS	16384×1	70	70	+5	25m/0.15	20		●	●		2167	147
		HM6167-6			85	85					●	●		2167-6	147
		HM6167-8			100	100					●	●		2167-8	147
		HM6167L			70	70		5μ/0.15				●			150
		HM6167L-6			85	85						●			150
		HM6167L-8			100	100						●			150
Dynamic	16k-bit	HM4716A-1	NMOS	16384×1	120	320	+12, +5, −5	0.35	16		●	●			156
		HM4716A-2			150	320					●	●		MK4116-2	156
		HM4716A-3			200	375					●	●		MK4116-3	156
		HM4716A-4			250	410					●	●		MK4116-4	156
		HM4816A-3	NMOS	16384×1	100	235	+5	11m/0.15	16		●	●		2118-3	167
		HM4816A-3E			105	200					●	●			167
		HM4816A-4			120	270					●	●		2118-4	167
		HM4816A-7			150	320					●	●		2118-7	167
	64k-bit	HM4864-2	NMOS	65536×1	150	270	+5	20m/0.33	16		●	●			175
		HM4864-3			200	335					●	●			175
		HM4864A-12*			120	230		20m/0.275			●	●			185
		HM4864A-15*			150	260					●	●			185
		HM4864A-20*			200	330					●	●			185

* Preliminary　　△HM6116LP Series: 10 μW

** The package codes of P, G, C, and FP are applied to the package materials as follows.
P : Plastic DIP, G : Cerdip, C : Side-brazed Ceramic DIP, FP : Small Sized Flat Package.

●MOS ROM

Program	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns) max	Supply Voltage (V)	Power Dissipation (W)	Package*** Pin No.	C	G	P	Replacement	Page
Mask	32k-bit	HN46332	NMOS	4096×8	350	+5	0.25	24			●		192
	64k-bit	HN48364		8192×8	350		0.225	24			●		194
	128k-bit	HN43128	CMOS	16384×8 32768×4	6000		3m	28			●		196
		HN613128*		16384×8	250		5μ/0.1	28			●		198
	256k-bit	HN61256		32768×8 65536×4	3000		3m	28			●		200
U. V. Erasable & Electrically	16k-bit	HN462716	NMOS	2048×8	450	+5	0.555	24	●	●		2716	202
		HN462716-1			350		0.555			●		2716-1	206
		HN462716-2			390					●		2716-2	206
	32k-bit	HN462532	NMOS	4096×8	450	+5	0.858	24	●	●		TMS2532	210
		HN462532-2			390					●			210
		HN462532L			450		0.543			●		TMS25L32	214
		HN462732	NMOS	4096×8	450	+5	0.788	24	●	●		2732	217
		HN462732-2			390					●			217
		HN482732A-20**	NMOS	4096×8	200	+5	—	24		●		2732A-2	221
		HN482732A-25**			250					●		2732A	221
		HN482732A-30**			300					●		2732A-3	221
	64k-bit	HN482764*	NMOS	8192×8	250	+5	0.555	28	●	●		2764	222
		HN482764-3*			300				●	●		2764-3	222
		HN482764-4			450				●	●			225
Electrically Erasable	16k-bit	HN48016*	NMOS	2048×8	350	+5	0.3	24			●		228

* Preliminary
** Under development
*** The package codes of P, G, and C are applied to the package materials as follows.
P : Plastic DIP, G : Cerdip, C : Side-brazed Ceramic DIP

■TYPICAL CHARACERISTICS OF BIPOLAR MEMORY

●Bipolar RAM

Level	Total Bit	Type No.	Organi-zation (word × bit)	Output	Access Time (ns) max	Supply Voltage (V)	Power Dissipation (mW/bit)	Package** Pin No.	F	G	P	Replacement	Page
ECL 10k	256-bit	HM2105	256×1	Open Emitter	35	−5.2	1.8	16		●		F10410	234
		HM2106			15		1.8			●			238
		HM10414			10		2.8			●		F10414	242
		HM10414-1			8					●			242
	1k-bit	HM2110	1024×1		35		0.5			●		F10415	246
		HM2110-1			25					●		F10415A	246
		HM2110-2			20					●			246
		HM2112			10		0.8			●			250
		HM2112-1			8					●			250
		HM10422	256×4		10		0.8	24		●		F10422	255
	4k-bit	HM10470	4096×1		25		0.2	18		●		F10470	260
		HM10470-1			15					●			260
		HM10474	1024×4		25		0.2	24		●		F10474	265
ECL 100k	1k-bit	HM100415*	1024×1		10	−4.5	0.6	16		●		F100415	270
		HM100422	256×4		10		0.8	24	●	●		F100422	273
	4k-bit	HM100470	4096×1		25		0.2	18		●		F100470	276
		HM100474	1024×4		25		0.2	24	●	●		F100474	279
TTL	256-bit	HM2504	256×1	Open Collector	55	+5	1.8	16		●		93411	284
		HM2504-1			45					●		93411A	284
	1k-bit	HM2510	1024×1		70		0.5			●			288
		HM2510-1			45					●		93415	288
		HM2510-2			35					●		93415A	288
		HM2511		3-state	70		0.5			●			292
		HM2511-1			45					●		93425	292

●Bipolar PROM

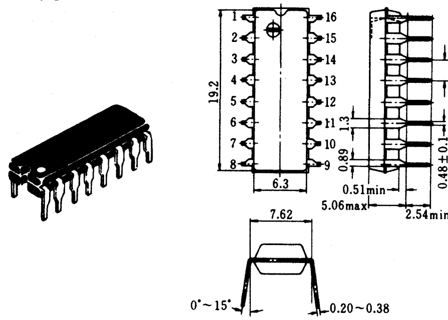
Level	Total Bit	Type No.	Organi-zation (word × bit)	Output	Access Time (ns) max	Supply Voltage (V)	Power Dissipation (mW)	Package** Pin No.	F	G	P	Replacement	Page
TTL	4k-bit	HN25044	1024×4	Open Collector	50	+5	500	18		●		82S136	298
		HN25045		3-state						●		82S137	298
	8k-bit	HN25084	2048×8	Open Collector	60		550	18		●		82S184	303
		HN25085		3-state						●		82S185	303
		HN25084S*		Open Collector	50		550			●			306
		HN25085S*		3-state						●			306
		HN25088	1024×8	Open Collector	60		600	24		●		82S180	309
		HN25089		3-state						●		82S181	309
		HN25088S*		Open Collector	50		600			●			312
		HN25089S*		3-state						●			312
	16k-bit	HN25168S*	2048×8	Open Collector	60		600	24		●		82S190	315
		HN25169S*		3-state						●		82S191	315

* Preliminary
** The package codes of F, G, and P are applied to the package material as follows.
F : Flat Package, G : Cerdip, P : Plastic DIP

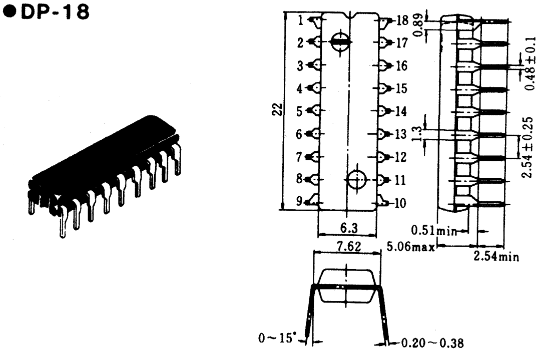
■PACKAGING INFORMATION (Dimensions in mm)

●DUAL-IN-LINE PLASTIC

●DP-16



●DP-18



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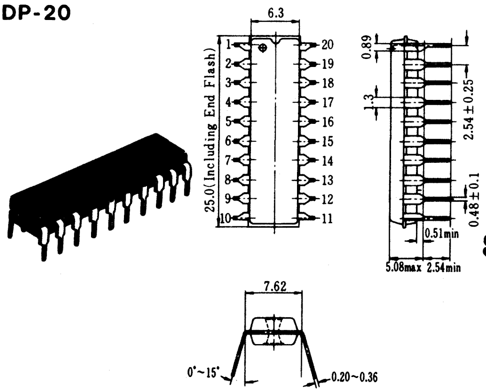
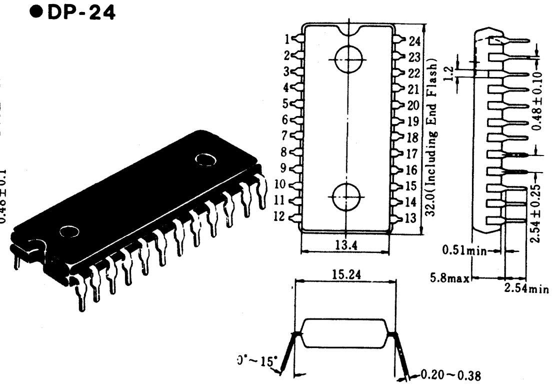
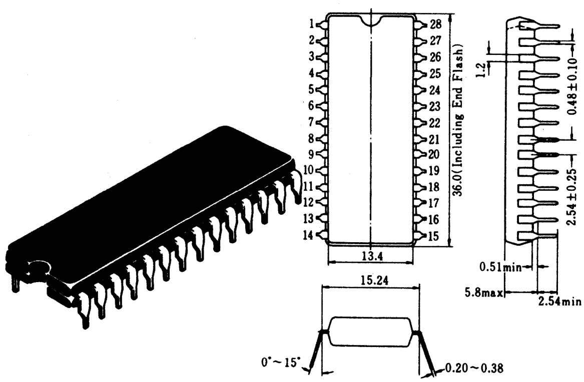


●DP-24



●DP-28

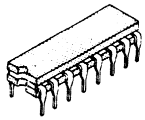


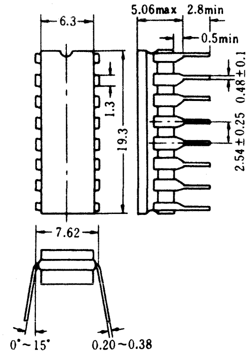
Applicable ICs

DP-16	HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4, HM4816AP-3, HM4816AP-3E, HM4816AP-4, HM4816AP-7, HM4864P-2, HM4864P-3, HM4864AP-12, HM4864AP-15, HM4864AP-20
DP-18	HM472114AP-1, HM472114AP-2, HM472114P-3, HM472114 P-4, HM4334P-3, HM4334P-4, HM4334P-3L, HM4334P-4L, HM6148P, HM6148P-6, HM6148LP, HM6148LP-6, HM4315P, HM6147P, HM6147P-3, HM6147LP, HM6147LP-3, HM6147HP-35, HM6147HP-45, HM6147HLP-35, HM6147HLP-45
DP-20	HM6167P, HM6167P-6, HM6167P-8, HM6167LP, HM6167LP-6, HM6167LP-8
DP-24	HM6116P-2, HM6116P-3, HM6116P-4, HM6116LP-2, HM6116LP-3, HM6116LP-4, HM6117P-3, HM6117P-4, HM6117LP-3, HM6117LP-4, HN46332P, HN48364P, HN48016P
DP-28	HN43128P, HN613128P, HN61256P

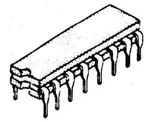
● CERDIP

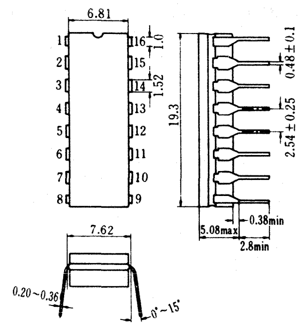
● DG-16



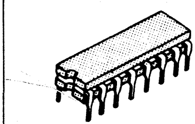


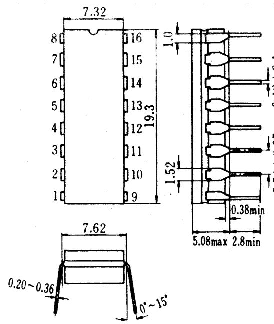
● DG-16A



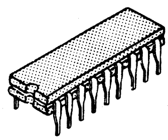


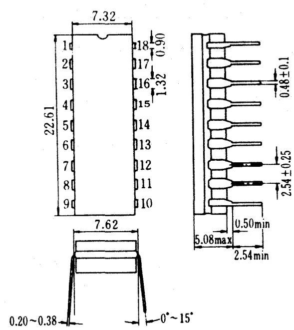
● DG-16B



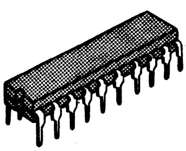


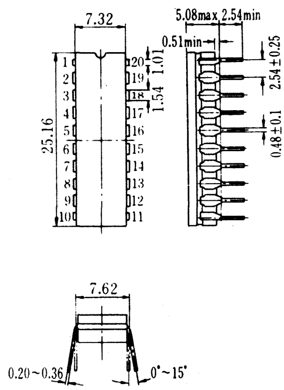
● DG-18



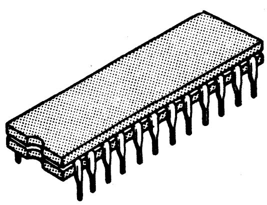


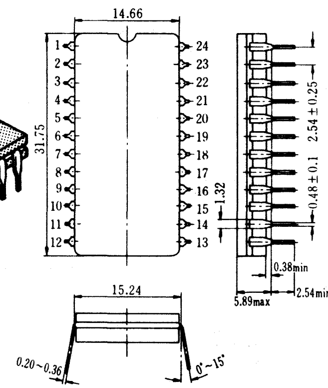
● DG-20



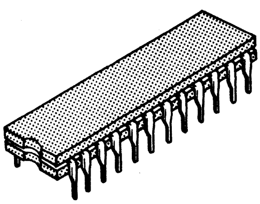


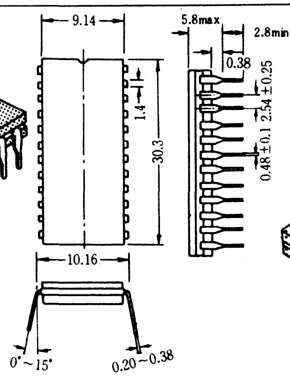
● DG-24





● DG-24A





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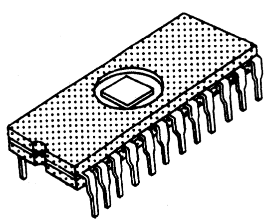
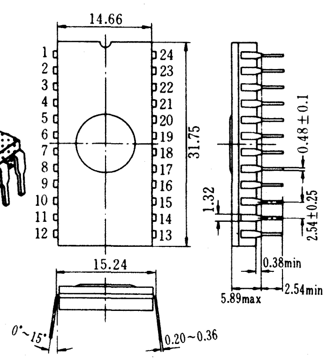
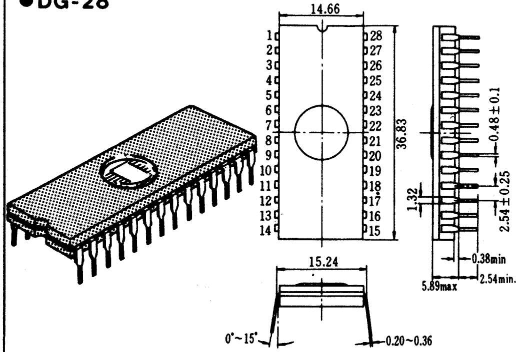




●DG-28

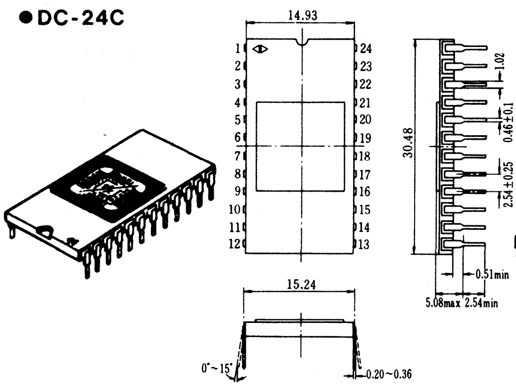


Applicable ICs

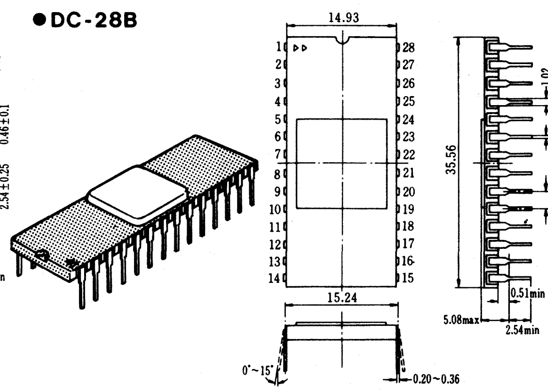
DG-16	HM2105, HM2106, HM10414, HM10414-1, HM2504, HM2504-1, HD2912
DG-16A	HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM2110, HM2110-1, HM2110-2, HM2112, HM2112-1, HM100415, HM2510, HM2510-1, HM2510-2, HM2511, HM2511-1, HD2916, HD2923
DG-16B	HM4816A-3, HM4816A-3E, HM4816A-4, HM4816A-7, HM4864-2, HM4864-3, HM4864A-12, HM4864A-15, HM4864A-20
DG-18	HM472114A-1, HM472114A-2, HM472114-3, HM472114-4, HM4334-3, HM4334-4, HM6148, HM6148-6, HM6147, HM6147-3, HM6147H-35, HM6147H-45, HM10470, HM10470-1, HM100470, HN25044, HN25045, HN25084, HN25084S, HN25085, HN25085S
DG-20	HM6167, HM6167-6, HM6167-8
DG-24	HM6116-2, HM6116-3, HM6116-4, HM6116L-2, HM6116L-3, HM6116L-4, HN25088, HN25088S, HN25089, HN25089S, HN25168S, HN25169S
DG-24A	HM10422, HM10474, HM100422, HM100474
DG-24B	HN462716G, HN462716G-1, HN462716G-2, HN462532G, HN462532G-2, HN462532GL, HN462732G, HN462732G-2, HN482732AG-20, HN482732AG-25, HN482732AG-30
DG-28	HN482764G, HN482764G-3, HN482764G-4

● SIDE-BRAZED DIP

●DC-24C



●DC-28B

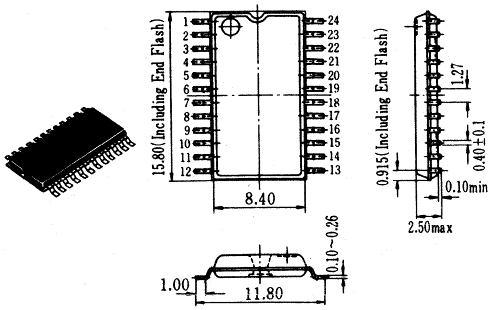


Applicable ICs

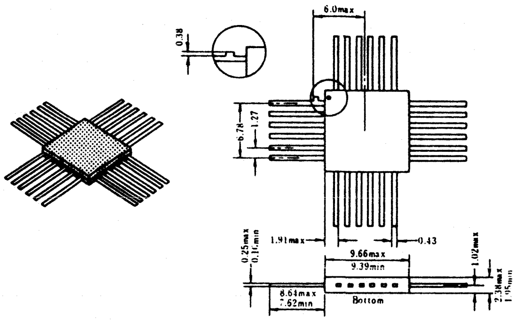
DC-24C	HN462716, HN462532, HN462732
DC-28B	HN482764, HN482764-3, HN482764-4

●Flat Package

●FP-24



●FG-24



Applicable ICs

FP-24	HM6116FP-2, HM6116FP-3, HM6116FP-4 HM6116LFP-2, HM6116LFP-3, HM6116LFP-4, HM6117FP-3, HM6117FP-4, HM6117LFP-3, HM6117LFP-4
FG-24	HM100422, HM100474

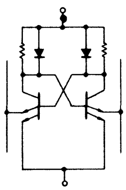
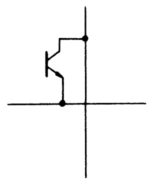
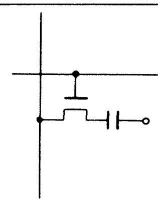
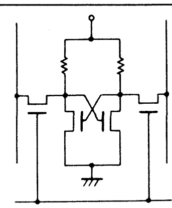
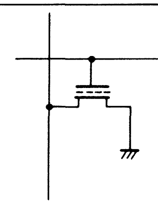
1. STRUCTURE

IC memories are structurally classified into bipolar type and MOS type. The former has a characteristic of an extremely high speed. Bui it is a comparatively small capacity and on the other hand, the latter features a large capacity. These IC memories are utilized by effectively taking the most of their respective characteristics.

Flows from designing, manufacturing and up to inspection for both Bipolar and MOS type IC memories are established under a unified concept, design and inspection standards. Therefore stable results concerning their reliability have been obtained with these IC memories, regardless of differences in the circuit design, pattern, layout, degree of integration, etc.

From its characteristics, the memory LSI is integrated in high density by unit patterns called "cell" and it is not exaggeration to say that they are produced in the most advanced semiconductor manufacturing technologies. To get the high reliability of such a memory which has been subjected to rapid technological advances, know-hows based on past experience from the design stage of a cell are incorporated. Farther to evaluated reliability of each respective technology applied. Reliability evaluation using TEG (Test Element Group), etc. is carried out. Examples of cell circuits of the Bipolar memory and MOS memory are shown in Table I.

● Table 1 Examples of Basic Cell Circuit of IC Memories

Classification	Bipolar memory (RAM)	Bipolar memory (PROM)	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Microcomputer control use	Main memory of computer, microcomputer memory		For microcomputer control
Example of basic cell circuit					

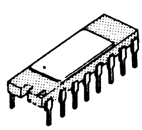
IC memory chips produced in the latest technologies are sealed in different packages. Ceramic package, Cerdip (glass-sealed type) and Plastic package are the current major IC packages. Also such packages as LCC (Leadless Chip Carrier) for high package density and SO (Small Outline) package are now under development.

Ceramic and Cerdip versions, with their hermetically sealed structure, are suitable to the equipment requiring high reliability. Plastic version, the leading semiconductor package, is applied to various kinds of equipment. Hitachi Plastic package has been improved to the close reliability level as the hermetically sealed devices. Table 2 shows examples of IC memory package outlines.

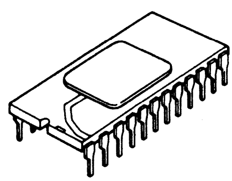
● Table 2 Examples of IC Memory Package Outlines

■ Ceramic DIP

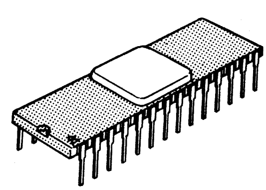
● 16 Pin

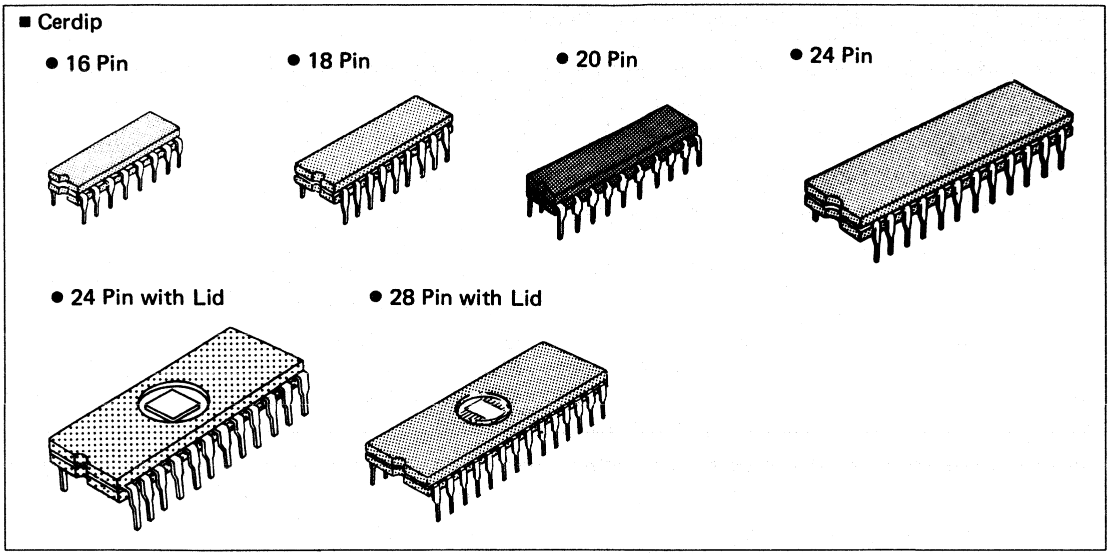


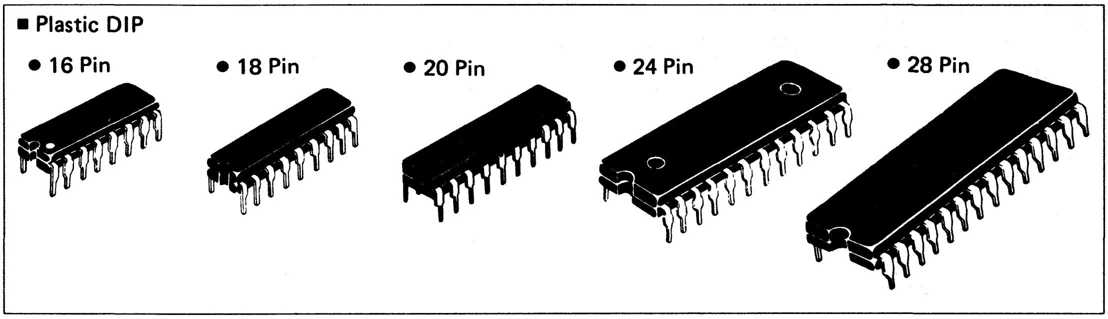
● 24 Pin



● 28 Pin







2. RELIABILITY DATA Results of reliability tests are listed below.

2-1 Reliability test data on Bipolar memories

The reliability test data on the Bipolar memories are shown in Tables 3 and 4. Since they are manufactured under the aforementioned standardized design rules and quality control, there is no difference in reliability among various types. In addition, it can be said that the greater the capacity, the higher the reliability per bit.

● Table 3 Results on Bipolar Memory Reliability Tests (1)

Test item	Test condition	HM10470 (Cerdip)				HN25089 (Cerdip)			
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*
High-temperature (Operating)	Ta=125°C V_{EE}=−5.2V (RAM) V_{CC}=5.5V (ROM)	125	C.H. 4.0×10^5	0	1/hr 2.3×10^{-6}	36	C.H. 3.6×10^4	0	1/hr 2.6×10^{-6}
	Ta=150°C V_{EE}=−5.2V (RAM) V_{CC}=5.5V, tcyc=1μs (ROM)	80	2.7×10^5	0	3.4×10^{-6}	10	1.0×10^4	0	9.2×10^{-5}
High-temperature storage	Ta=200°C	27	2.7×10^5	0	3.4×10^{-5}	15	1.5×10^4	0	6.1×10^{-5}
	Ta=295°C	20	2.0×10^5	0	4.6×10^{-5}	15	1.5×10^4	0	6.1×10^{-5}

* Estimated failure rate with confidence level 60%

● **Table 4 Results on Bipolar Memory Reliability Tests (2)**

Test Item	Test condition	HM10470 (Cerdip)		HN25089 (Cerdip)	
		Samples	Failures	Samples	Failures
Temperature cycling	−65°C ~ 150°C, 10 cycles	120	0	45	0
Soldering heat	260°C 10 seconds	22	0	22	0
Thermal shock	0°C ~ 100°C 10 cycles	36	0	22	0
Mechanical Shock	1,500G, 0.5ms Three times each for X, Y, and Z	30	0	22	0
Variable frequency	100 ~ 2,000Hz, 20G Three times each for X, Y and Z	40	0	22	0
Constant-accelaration	20,000G 1 minute each for X, Y and Z	40	0	22	0

2-2 Reliability test data on MOS memories

The reliability test data on the MOS memories are shown in Tables 5, 6 and 7. In these tables, data are shown on representative types of HM4864 (64K DRAM), HM4716AP (16K DRAM), HM6116P (16K SRAM), HM6147P (4K SRAM), HN462732, HN462532 (32K EPROM), HN462716 (16K EPROM).

● **Table 5 Results on MOS Memory Reliability Tests (1)**

Test item	Test condition	HM4864 (Ceramic)				HN462532/HN462732 (Cerdip)				Remarks
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*	
High-temperature dynamic operation	Ta=125°C V_{CC}=5.5V t_{cyc}=3μs	1872	C.H. 3.33×10^6	3*1	1/hr 1.25×10^{-6}	100	C.H. 1.0×10^5	0	1/hr 9.2×10^{-6}	*1 Oxide failure x 2 Unknown x 1
High-temperature storage	Ta=200°C	20	4.0×10^4	0	2.3×10^{-5}	140	1.4×10^5	0	6.6×10^{-6}	
High-temperature storage	Ta=259°C	–	–	–	–	100	5.0×10^4	0	1.8×10^{-5}	
High-temperature storage	Ta=295°C	–	–	–	–	100	4.2×10^4	1*2	4.8×10^{-5}	*2 Data disappearance

* Estimated failure rate with confidence level 60%

● **Table 6 Results on MOS Memory Reliability Tests (2)**

Test item	Test condition	HM4716AP (Plastic)				HM6116P/HM6147P (Plastic)				Remarks
		Samples	Total component hours	Failures	Failure rate*	Samples	Total component hours	Failures	Failure rate*	
High-temperature dynamic operation	Ta=125°C V_{DD}=13.2V (NMOS) V_{CC}=5.5V (CMOS) t_{cyc}=3μs	2330	C.H. 3.46×10^6	6*1	1/hr 2.12×10^{-6}	1216	C.H. 1.90×10^{-6}	3*2	1/hr 2.19×10^{-6}	*1 Oxide failure x 6 *2 Oxide failure x 1 Electrostatic discharge x1 Unknown x 1
High-temperature storage	Ta=150°C	45	4.5×10^4	0	2.0×10^{-5}	20	2.0×10^4	0	4.6×10^{-5}	
High-temperature and high-humidity bias	Ta=85°C, RH=85% V_{DD}=12V (NMOS) V_{CC}=5.5V (CMOS)	3081	6.2×10^6	19*3	3.1×10^{-6}	630	1.3×10^6	4*4	4.0×10^{-6}	*3 Aluminium corrosion x 17 Unknown x 2 *4 Aluminium corrosion x 3 Unknown x 1

* Estimated failure rate with confidence level 60%.

● Table 7 Results on MOS Memory Reliability Tests (3)

Test item	Test condition	HM4864 (Ceramic)		HM4864 (Cerdip)		EPROM (Cerdip)		HM4716AP		HM6116P/ HM6147P	
		Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures
Temperature cycling	-65°C~RT~150°C 10 cycles	1208	0	260	0	50	0	–	–	–	–
Temperature cycling	-55°C~RT~150°C 10 cycles	–	–	–	–	310	0	7892	0	2080	0
Temperature cycling	-55°C ~ 150°C 1000 cycles	164	0	100	0	50	0	600	0	–	–
Thermal shock	-65°C ~ 150°C 15 cycles	22	0	60	0	72	0	190	0	–	–
Thermal shock	0°C ~ 100°C 15 cycles	–	–	–	–	197	0	138	0	60	0
Soldering heat	260°C, 10 seconds	22	0	22	0	22	0	128	0	60	0
Mechanical shock	1,500G, 0.5ms	22	0	38	0	38	0	–	–	–	–
Variable frequency	20~2,000Hz, 20G	22	0	38	0	38	0	–	–	–	–
Constant-acceleration	20,000G	22	0	38	0	38	0	–	–	–	–

2.3 Change of electrical characteristics under endurance test for IC memories

The degradation of I_{CBO} of the cell transistor, degradation of h_{FE}, etc., can be considered as main factors in the internal elements for reliability of Bipolar memories. In actual element designing, however, it has been designed to operate in the range at which these degradations do not happen. Therefore changes of electrical characteristics including access time are not observed.

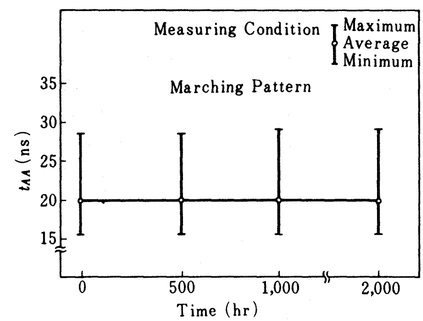
Time dependence in access time for HM10470 is shown in Fig. 1.

Fig. 1 Example of Change in Bipolar Memory Characteristics

Example	
Device name	HM10470
Test condition	Ta=125°C, V_{EE}=-5.2V
Failure criteria	t_{AA}=25ns
Failure mechanism	Surface degradation

Results:
Access time (t_{AA}) is stabilized and is within the failure criteria.

Example of time change in access time for Bipolar memory



V_{TH} is a basic parameter in the MOS memories, however, it has been confirmed there is not any shift in V_{TH} for practical usage because we have applied surface stabilizing technique, clean process, etc.

In case of dynamic RAM which needs refresh cycle, refresh time is also stabilized owing to the above-mentioned process. Time dependence of Vcc min and t_{REF} characteristics for the 64K DRAM are shown in Fig. 2 and 3.

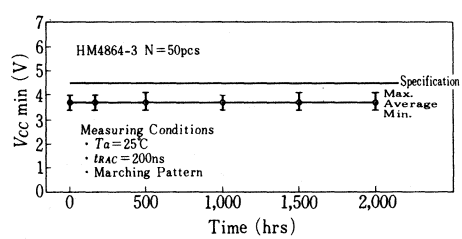


Fig. 2 V_{CC} min time dependence in dynamic operation test at 125°C

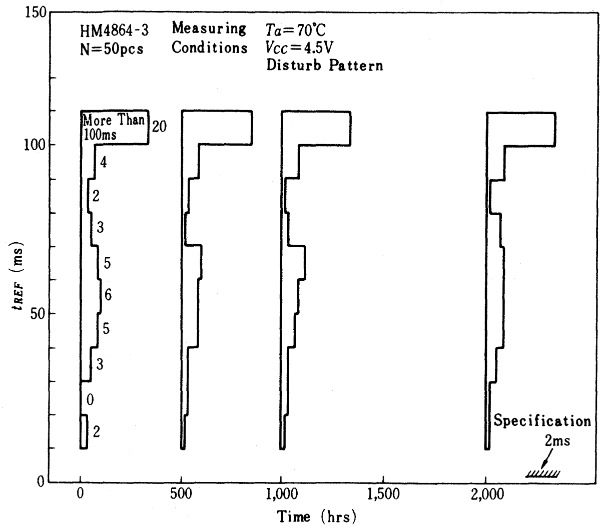


Fig. 3 Time dependence in refresh time (t_{REF}) in dynamic operation test at 125°C

2.4 Classification of failure modes

Examples of failures happened in the field are shown in Fig. 4 and 5. Since memory LSIs generally require the most fine processing in semiconductor manufacturing technology, the percentage of failures resulting from pinholes, photoresist defects, foreign materials, etc., is tending to increase. To eliminate the latent defects which are generated in these manufacturing processes, we are constantly improving these processes, and performing burn-in screening under high temperature for all memories. In addition, since the analysis of failures in the field can result in important feedback to improve their design and manufacturing, we are always exerting our efforts to collect customer process data and field data with the aim of further establishing their high reliability.

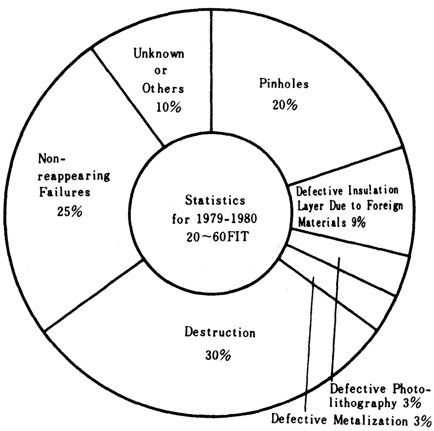


Fig. 4 Classification of Failure Modes of Bipolar Memory in the field

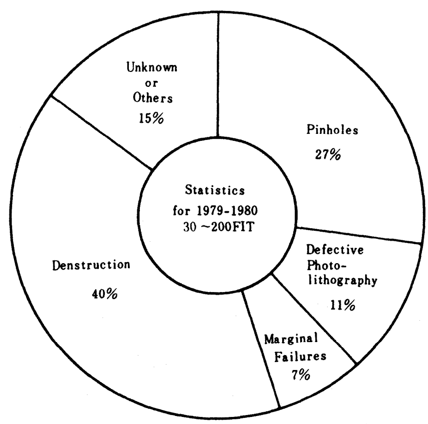
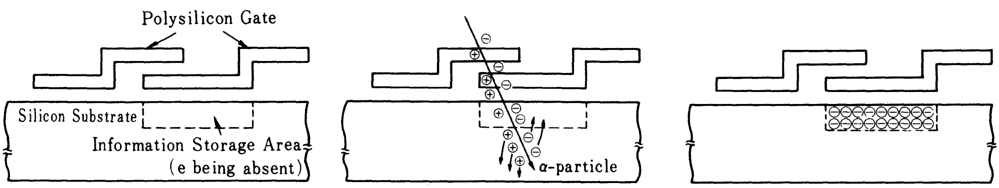


Fig. 5 Classification of Failure Modes of MOS Memory in the field

3. SOFT ERROR

3.1 Soft Error Mechanism

As mentioned before, IC memories have been increasingly miniaturized. Miniaturization, which means reduction of the horizontal plane dimensions as well as the vertical dimensions, causes signal level on the chip and storage charge of dynamic memories to be also decreased. An obstacle lying before miniaturization is soft error. Soft errors can be characterized as "transitory failures in which normal memory operation can be recovered by reprogramming information." Soft errors are caused by α-particles emitted from U and T_H contained in the packaging materials. As memory chips are exposed to α-particles, a great deal of electron-hole pairs are induced in Si substrate. These induced electrons cause memory information reversion. Fig. 6 shows the mechanism of information reversion in NMOS dynamic memory by α-particles. In case of NMOS dynamic memory, negative voltage is applied to the Si substrate. Therefore, positive holes are drawn by substrate, and only electrons cause information reversion (from information "1" to "0") of memory cell. Fig. 6 shows misoperation seen in memory cell. Such a failure mode, which is defined as "Memory cell mode of soft errors," is distinguished from "Bit line mode." "Bit line mode" of soft errors is shown in Fig. 7. As information in memory cell is read out on bit line, bit line potential changes depending on memory cell information. The changing value is very small (several 100 mV), and compared with standard potential (potential read out from dummy cell), it is amplified by sense amplifier. If bit line is exposed to α-particles during the very short period between read-out from memory cell and amplification by sense amplifier, bit line potential decreases. And as it becomes less than standard potential, misoperation from information "0" to "1" will take place. On the other hand, with decrease of standard potential, misoperation from information "1" to "0" is seen. Both are called "Bit line mode" because errors appear at irradiation of α-particles. Soft error dependence on cycle time is shown in Fig. 8.

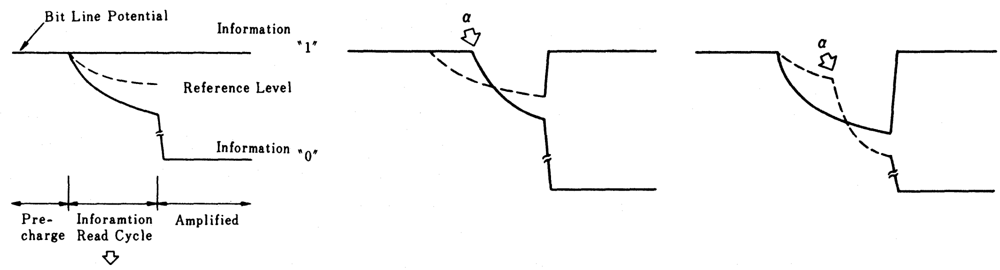


(a) Memory information at "1" (Electrons are absent) (1 Transistor type memory cell)

(b) Incident α-particle generate a large quantity of electron-hole pairs. Generated electrons enter the information storage area and holes are drawn to the substrate power supply.

(c) Inversion of memory information from "1" (electrons "absent") to "0" (electrons "filled")

Fig. 6 Misoperation in Memory Cell



(a) **Read out memory information into bit line**

(b) **Inversion of information from "1" to "0" (fall of "1" potential)**

(c) **Inversion of information from "0" to "1" (fall of standard potential)**

Fig. 7 Misoperation on Bit Line

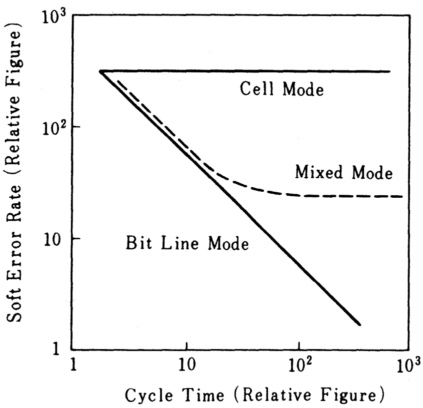


Fig. 8 Soft Error Rate's Dependence on Cycle Time

Actual products will have three types of failure modes, that is, cell mode, bit line mode and mixture of both modes. Soft error mechanism of static MOS memories and of bipolar memories are different from the above-mentioned mechanism in dynamic MOS memories.

In case of static memory, certain level of current always flows through the cell in order to retain the data in flip-flop circuit. When partial current induced by α-particles exceeds the retention current, misoperation occurs because of reversion of flip-flop circuit.

3.2 Examples of soft error preventive measures in products

At the initial stage of the 64K DRAM development, its soft error rate was estimated from accelerated irradiation test data to be higher than the expected design value. Hitachi has performed the following soft error preventive measures.

1) Selection of packaging materials which emit a minimal number of α-particles.
2) Application of chip coating technology to prevent the α-particles.
3) Use of circuitry and layout technology with inherent ability to resist α-particles.

Owing to these corrective measures, soft errors in 64K DRAM have reached a practically acceptable level. Preventive measures applied for 64K DRAM are also applied to other types. 16K DRAM with single power supply 5V family, for which chip coating was originally used, no longer requires this coating because of remarkable improvement by the third measure.

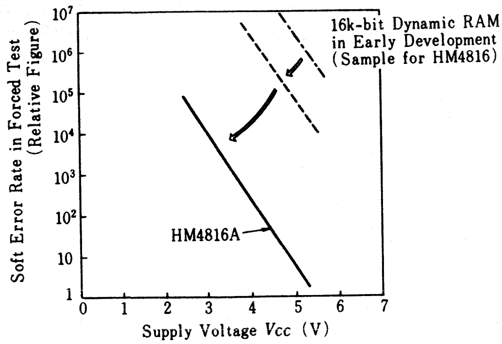


Fig. 9 Example of Soft Error Improvement on 16K-bit Dynamic RAM

3.3 Request for soft error preventative measures in system equipment

Thus our efforts to reduce soft errors have resulted in almost trouble-free memories. System reliability can be more improved by supplying some functions, that is, ECC device for lage memory system and parity bit for small one.

4. RELIABILITY CLASSIFICATION

In designing IC memories, Hitachi classifies memory reliability by their application and controls the flows of design, production and test. Reliability can be roughly classified as follows:

(I) For large scale computers and electronic exchangers

(II) For important parts for auto-motive application

(III) General communication-industrial use

In using our products, therefore, we would like you to consider the classification of the application. Especially, when you are going to apply our memories to any special equipment, please do not hesitate to consult our sales engineering staff.

A variety of IC memories of high-spped, high-power and static lower power dissipation CMOS have been developed and commercially available, which allows an electronics designer to properly select the one best suited for a particular application. However, he must be familiar with the advantages and disadvantages of the devices to make the optimum selection and to prevent them from malfunctioning or, in the worst case, from breaking down. Precautions for handling IC memories given below will help the electronics designers to work out their optimum circuit designs.

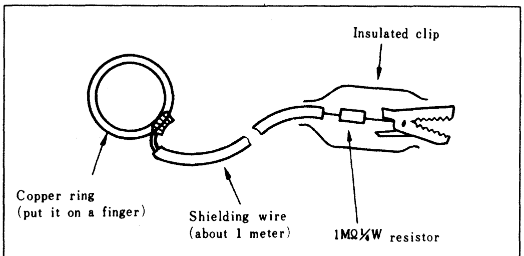
1. BIPOLAR IC MEMORY

1.1 Prevention of static electricity

Bipolar ICs have been considered to have high resistance to the static electricity than MOS ICs. However, the presently available high speed IC, represented by bipolar memories, must be provided with a suitable preventive measure against the static electricity. Because their diffused junctions have become thinner than the conventional taypes, in order to perform higher capability. Take note of the following points.

(1) Keep all terminals of a device in the conductive mat during transportation and storage to keep them at the same potential. A conductive mat called "MOSPAK" is commercially available. Unless otherwise specially stated, all HITACHI IC memories will be shipped in our conductive mats. Store them as they are.

(2) When handling by hand IC memories for inspection or connection, his finger must be grounded as shown in Fig. 1. Do not forget to insert a 1M ohm resistor to protect him against an electric shock.



(3) It is advisable to control the ambient relative humidity at about 50 per cent to prevent the occurrence of static electricity.

(4) It is also recommendable to wear cotton clothes instead of the ones made of synthetic fabrics to prevent the static electricity from occurring.

(5) It is desirable to ground the soldering iron tips. Use a low voltage soldering iron (12 or 24V), if possible.

(6) When IC memories mounted on the circuit boards are shipped, it is preferable to pack them with conductive mats.

1.2 Cooling down

A bipolar memory will dissipate about 0.5 W of power notwithstanding it is operated or not operated. For instance, a 4K byte memory card consisting of 36 peices of HM2510 devices will dissipate about 20 Watts. Since the heat generated by such a circuit board is too great to be removed by the natural convection, a forced air cooling system having a capability of 2.5 m/s or more air blow must be installed. A large memory system must be installed in a sealed housing which has a pair of air inlet and outlet.

1.3 Preventive measures for reverse insertion

If a device is reversely connected, an excessive current will flow to burn the connection leads to the memory chip resulting in breakdown of the device, because its V_{CC} and ground terminals are symmetically positioned. Locate the pin No. 1 which is indicated by a mark on the top surface of each device and provide the device with correct connection.

2. MOS IC MEMORY

2.1 Prevention of static electricity

Similar to bipolar IC memories, suitable preventive measures should be taken for MOS IC memories by referring to paragraph 1.1.

2.2 Absorption of power source noise

The source current level flowing in the dynamic memory during the time of access is considerably different from that of stand by. Although the current difference is quite effective to save the power consumption, the current spike may be developed into the power source noise. Since all MOS IC memories are, in general, accessed while being refreshed, it is recommended to insert large capacitors (a 10 μF capacitor for every 9 pieces of 16K-bit HM4716A, for example) as well as a 0.1 μF capacitor having good high-frequency characteristics for each memory. Needless to say, it is very important to reduce the power circuit impedance when designing.

2.3 Current spike in V_{BB} power

The V_{BB} power is necessary for maintaining the IC memory function in the reverse bias and the current does not generally exceed the level of the reverse leakage current. However, in order to prevent an accidental current spike which is sharply formed in either positive or negative phase by the rise or fall clock pulse at the time of access, use a 0.1 μF capacitor for every 2 or 3 memories for absorbing such noises.

2.4 Clock drive ICs

The TTL to MOS clock drive ICs have special designs so that they are capable of quick increase in the capacitive load. If a ground wire short-circuits either V_{DD} or V_{CC} which appear in the Pin No. 1 and No. 16 respectively, when the device is at high level, the device may be broken down. Carefully eliminate such possibility beforehand.

2.5 Power application sequence

It is advisable to design the circuits so that power is applied in the sequence of V_{BB}, V_{DD} and V_{CC} and interrupted in the reverse sequence, here the reverse bias V_{BB} is applied first and interrupted last.

It may be impossible for some small-scaled systems to apply power in the above-mentioned sequence (for example, when the V_{BB} is supplied by a DC to DC converter). According to our experiments conducted in the under-mentioned test conditions, it has been proved that such a small-scaled system as to consist of 200 to 300 memory devices is not affected by he power application sequence.

Power application sequence test for N MOS IC

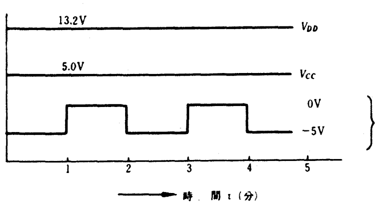
1.) Test method

(1) Ambient temperature: 25°C

(2) Power voltage: V_{DD}=13.2V, V_{CC}=5.0V, V_{IH}=5.0V

(3) Operation mode: AC operation ("0" to "16383" all bits scanning). t_{cyc}=10 μs Read modify write operation

(4) V_{BB} power: ON (1 min.) – Floating (1 min.)



2.) Test results

Type No.	Number of cycles	Number of sample	Number of failures
HM4716A	2000 cycles	50	0

2.6 Assessment of the memory system design

It is quite effective to obtain the power margin curves (shmoo curve) for evaluating the memory system designs (timing margin or adaptability to the peripheral circuits). Investigate the V_{BB} and V_{DD} power behaviors by gradually varying their levels, and the ones which are closer to the margine shown by the memory device itself can be judged to be better than others.

2.7 Overhead parity bit

Application of MOS IC static memory especially to microcomputers has been rapidly increasing due to the advantages that MOS static memory is operated by a single 5V power source and refreshing is not required.

There are some cases where all bits are used as the information bit without inclusion of any parity bit by some circuit designing reasons. It is, however, desirable to add parity bits to thoroughly avoid the memory error.

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality in Hitachi are to meet individual users' purchase purpose and quality required, and to be at the satisfied quality level considering general marketability. Quality reuired by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize the quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance morale for quality. In addition, quality required by users on semiconductor devices are going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

(1) Build the reliability in design at the stage of new product development.
(2) Build the quality at the sources of manufacturing process.
(3) Execute harder the inspection and reliability confirmation of final products.
(4) Make quality level higher with field data feed back.
(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as wel as performance and price.
It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely sude and execution of design standardization, device design (include process design, structure design), design review, reliability test are essential.

(1) Design Standardization
Establishement of design rule, and standerdization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices only except for in the case special requirements in function needed.

(2) Device Design
It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Site
Test site is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of Test Site are as follows;
   - Making clear about fundamental failure mode
   - Analysis of relation between failure mode and manufacturing process condition
   - Search for failure mechanism analysis
   - Establishment of QC point in manufacturing
2 Effectiveness of evaluation by Test Site are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competition power of products, the major purpose of design review is to insure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows;

(1) Description of the products based on specified design documents.
(2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub program of calculation, experiments, investigation, etc. will be carried out.
(3) Determine contents of reliability and methods, etc. based on design document and drawing.
(4) Check process ability of manufacturing line to achieve design goal.
(5) Discussion about preparation for production.
(6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.
(7) Reference of past failure experiences with similar devices, confirmation of method to provent them, and planning and execution of test program for confirmation of them. These study and decision are made using check lists made individually depending on the objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows;

(1) Problems in individual process should be solved in the process. Therefore, at final product stage, the potential failrue factors have been already removed.
(2) Feedback of information should be made to insure satisfied level of process ability.
(3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To insure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2.

The views on quality approval are as follows;

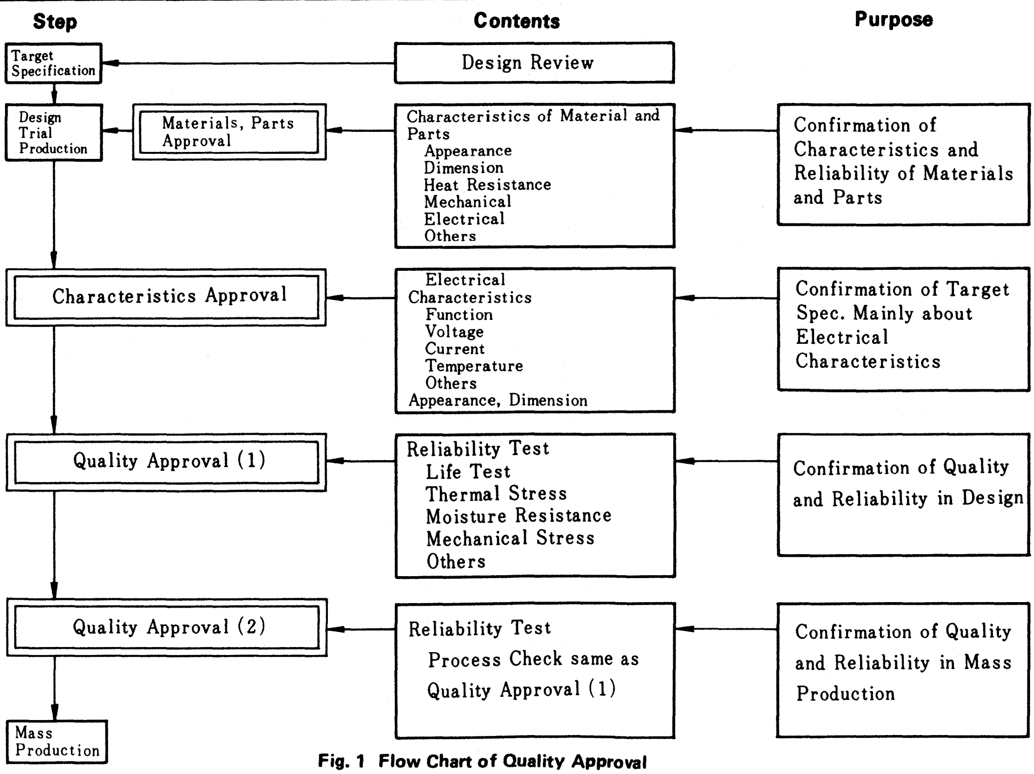


Fig. 1 Flow Chart of Quality Approval

(1) The third party executes approval objectively from the stand point of customers.
(2) Fully consider past failure experiences and information from field.
(3) Approval is needed for design change and work change.
(4) Intensive approval is executed on parts material and process.
(5) Study process ability and fluctuation factor, and set up control points at mass production.

Considering the views mentioned above, quality approval shown in Fig. 1 is executed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total function flow is shown in Fig. 2. The main points are described below.

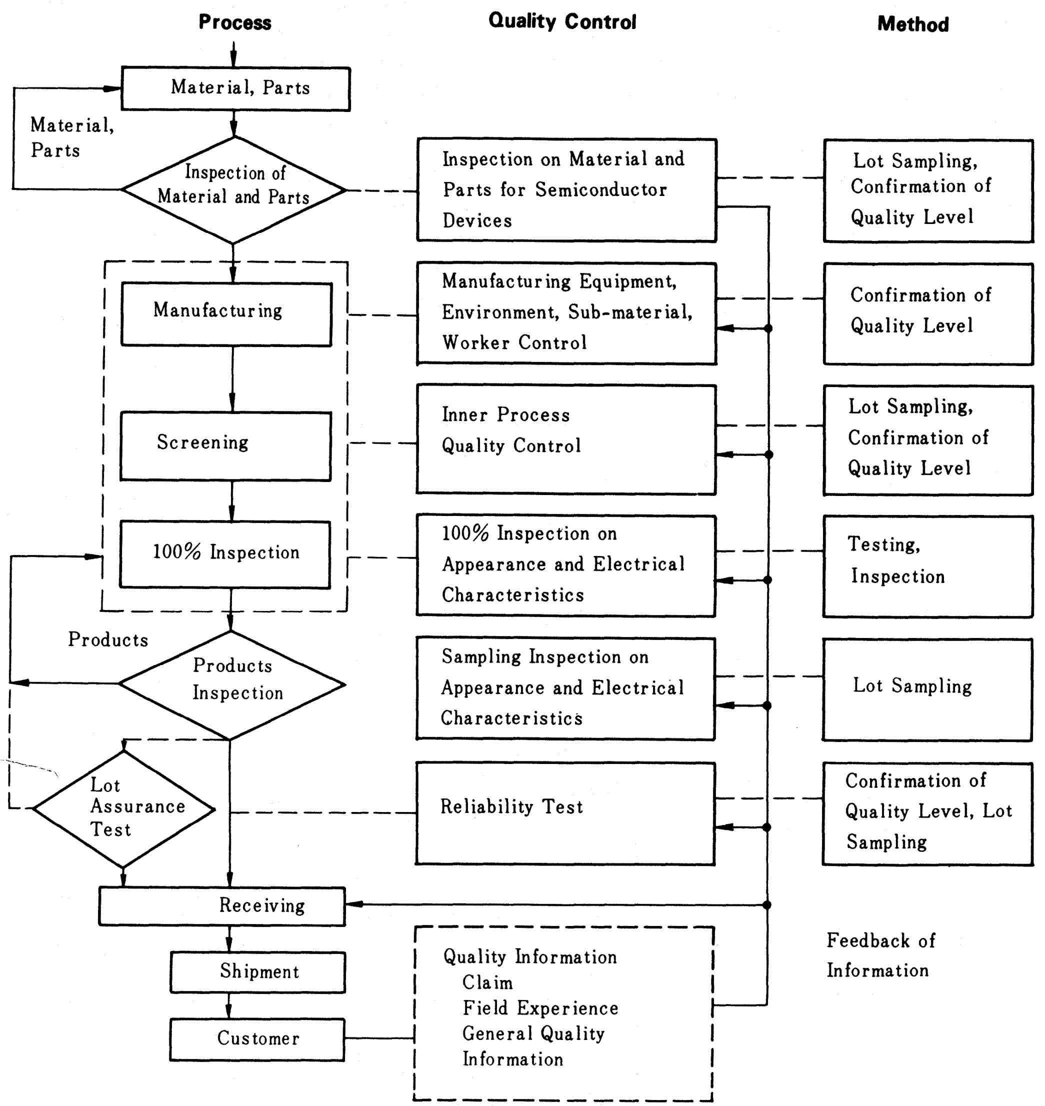


Fig. 2 Flow Chart of Quality Control in Manufacturing Process

3.3.1 Quality Control of Parts and Material

As tendency toward higher performance and higher reliability of semiconductor devices, is going, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

The other activities of quality assurance are as follows;

(1) Outside Vendor Technical Information Meeting
(2) Approval on outside vendors, and guidance of outside vendors
(3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

● Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments, circumstances and sub materials. The manufacturing inner process quality control is shown in Fig. 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and tighter inner process quality control is executed — rigid check in each process and each lot, 100% inspection pointed process to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semi-final products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of countermeasures
- Transfer of information about quality

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing equipments are extraordinary developing as higher performance devices are needed and improvement of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain prompt operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are checked one by one not to make any omission. As for adjustment and maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-materials

Quality and reliability of semiconductor device is highly affected by manufacturing process. Therefore, the controls of manufacturing circumstances — temperature, humidity, dust — and the control of submaterials — gas, pure water — used in manufacturing process are intensively executed. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, air-conditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating dust in room, falling dusts and dirtiness of floor.

Process	Control Point		Purpose of Control
Purchase of Material			
Wafer	Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
Surface Oxidation	Oxidation		Assurance of Resistance
Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
Photo Resist	Photo Resist		
Inspection on Photo Resist		Dimension, Appearance	Dimension Level
◇PQC Level Check			Check of Photo Resist
Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
Inspection on Diffusion		Gate Width	Control of Basic Parameters
◇PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	(V_{TH}, etc) Cleaness of surface, Prior Check of V_{IH} Breakdown Voltage Check
Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
Inspection on Evaporation			
◇PQC Level Check			
Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
Chip Scribe		Appearance of Chip	
Inspection on Chip Appearance			
◇PQC Lot Judgement			
Frame — Assembling	Assembling	Appearance after Chip Bonding Appearance after Wire Bonding	Quality Check of Chip Bonding Quality Check of Wire Bonding
◇PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
Inspection after Assembling		Appearance after Assembling	
◇PQC Lot Judgement			
Package — Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
◇PQC Level Check	Marking	Marking Strength	
Final Electrical Inspection			
◇Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
Appearance Inspection			
Sampling Inspection on Products			
Receiving			
Shipment			

Fig. 3 Example of Inner Process Quality Control

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.

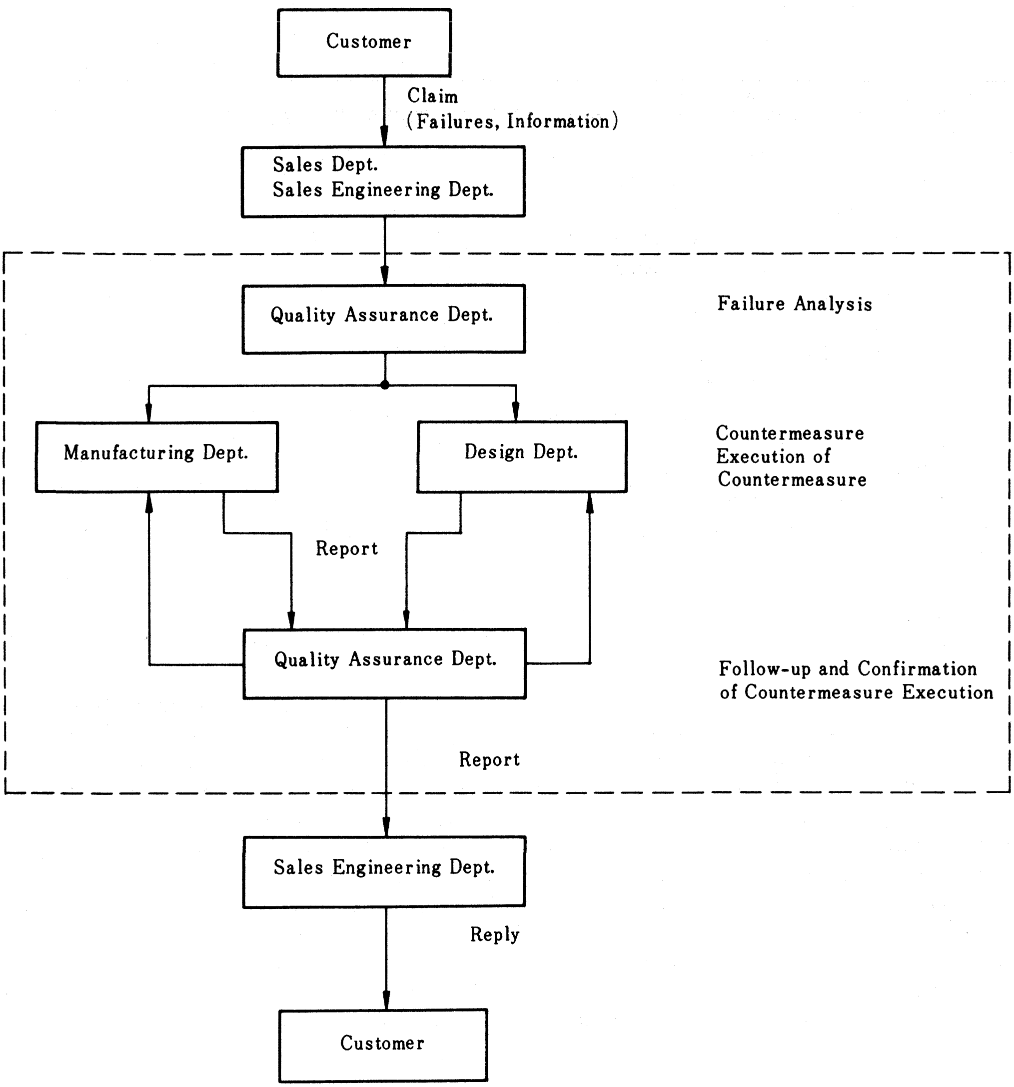


Fig. 4 Process Flow Chart of Field Failure

OUTLINE OF TESTING METHOD

1. Inspection Method

Compared to conventional core memories, all peripheral circuits such as the decoder circuit, write circuit, read circuit, etc., are contained within the IC memories. As a result, all works of assembling the parts and performing electrical inspection, which had been carried out by core memory manufacturers in the past, have be come to be incorporated as works of IC manufacturers. Consequently, the electrical inspection of the memory IC has been faced to a more systematic inspection method and conventional IC inspection facilities have become completely useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a comparatively simple DC parameter facility. However, when the address input becomes multiplexed as in 16K memory, even the generation of the function test pattern becomes a serious problem. In the memory IC inspection, its quality cannot be judged by only inspecting DC characteristics related to external pins. This is because numbers of transistors, etc., related to the DC characteristics of the pins only amount to 1/1000 of all element numbers within IC memories. The following various address patterns are proposed to inspect whether or not the internal circuits are functioning correctly.

(1) All "Low", all "High"
(2) Checker flag
(3) Stripe pattern
(4) Marching
(5) Galloping
(6) Walking
(7) Ping-pong

Although there are a lot of address patterns, only representative ones have been listed. These patterns are convenient for checking the mutual finterference of bits and sometimes are patterns with maximum power dissipation. Among the above-mentioned patterns, those of (1) to (4) are the socalled N patterns and these patterns are capable of checking IC memories of N bits with several sequences of N at most against the memory IC of N bits. Whereas, those of (5) to (7) are caled N^2 patterns and they need patterns several sequences of N^2.

A serious problem arises in using the N^2 patterns in a large-capacity memory, for example, a long period of about 30 minutes becomes necessary to perform inspection of the 16K memory with galloping pattern. Patterns from (1) (3) are comparatively simple and good methods, but they are not perfect against a failure in the decoder circuit. As the most simple pattern for inspecting the necessary memory function, there is a "Marching" pattern.

2. Marching Pattern

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits written in "0"s. The addressing method will be explained for a simple 16 bit memory as an example.

(1) Write "0" for all bits .... Fig. 1(a)
(2) Read "0" of 0th address and check that the read data is "0". Hereafter, the meaning of "Read" is "checking and judging the data".
(3) Write "1" in the 0th address .... Fig. I(b)
(4) Read "0" of 1st address
(5) Write "1" in 1st address
(6) Read "0" of nth address
(7) Write "1" in nth address .... Fig. 1(c)
(8) Repeat above procedures (6) and (7) up to the last. Finally, all data will become "1".
(9) Since all data are "1"s in this condition, replace "0" and "1" after procedure (2) and repeat once more up to procedure (8).

It is understood that 5N address patterns are necessary for the N bit memory in this method.

(a)

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

(b)

1	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0

(c)

1	1	1	1
1	1	1	1
1	1	0	0
0	0	0	0

Fig. 1 Addressing method for 16 bits memory in the Marching pattern

3. Generation of Marching Pattern

The method of generating the marching pattern and displaying failed bits of the memory on the Braun tube will be introduced. Fig. 2 shows the all block diagram. The address pattern is generated by using four synchronous 4 bit counters. All address patterns are shown in Fig. 4. This example, is for 16K bit memory, however, it can be easily understood that A14 which has a half frequency of the maximum address input A13 is the same as the data input.

The A15 signal together with the carrier signal of HD74161 is used to determinine the termination of the sequence.

As shown in Fig 2. In the read and write cycles after cleaning all bits addressing is twice the period of clearing. This switching is performed at the gate of the binary circuit following the reference pulse generating circuit.

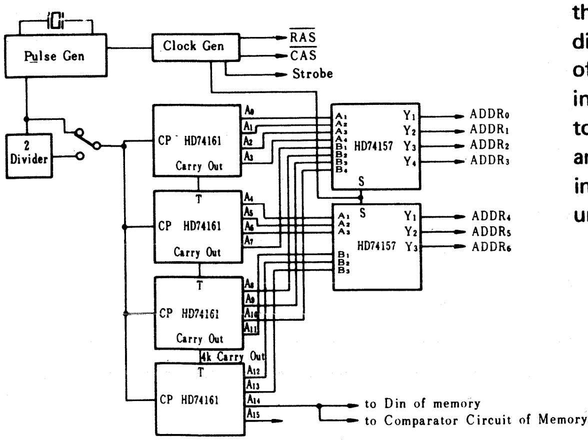


Fig. 2 Marching Pattern Generating Circuit

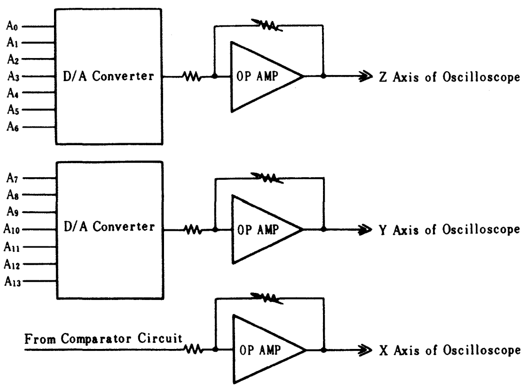


Fig. 3 Fail Bit Map Display Circuit

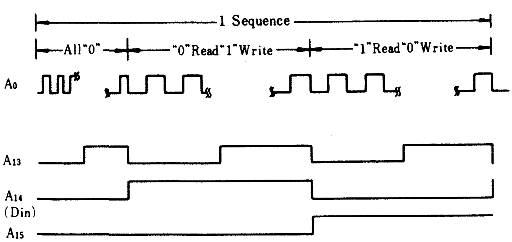
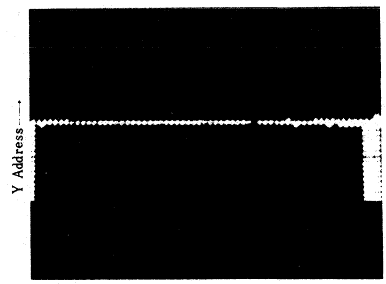
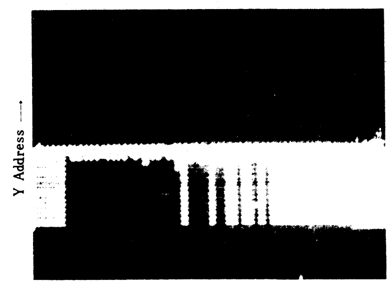


Fig. 4 Entire Pulse Relations

Input the output of HD74161 is input to the D/A converter and the output of D/A converter is connected to the oscilloscope to display → X-Y matrix. The output of the comparator circuit is connected to the Z axis and performs luminous intensity modulation. In this way, the fail bit map can be displayed on the CRT. Fig. 5 shows an example checking a voltage margin. By changing the power voltage V_{BB}, the increase and decrease of the failed bits can be well understood. The operation of the memory can be dynamically understood by displaying its operation on the CRT. The operation of the memory IC is extremely complicated differing from other TTLs, etc.. Its operation is not easy to understand by pulse waveform observation with an ordinary oscilloscope. The fail bit map as shown in Fig. 5 is extremely useful. It is capable of visually understanding the operation of memory IC.

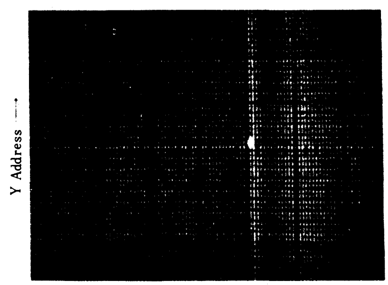


(a) V_{BB} −0.3V X Address →



(b) V_{BB} = −0.1V X Address →

Fig. 5 Example of Dependency of Fail Bit Map on V_{BB}



X Address →

Fig. 6 Example of 1 bit solid fail

4. Failure Mode

Generally, failure 70% ~ 90% of failures at users are of those called solid failure. This failure mode has no relation with access time, voltage margin and timing, and is not capable of reading from or writing to certain specified bits and is failure fixed to "0" or "1". An example of single bit solid failure is shown in Fig. 6. The convenient checker, previously mentioned as simple tester, is sufficiently capable of detecting such failures. Therefore, with the exception of special cases, it can be considered that the necessity of performing high-precision measurements such as those made by memory IC manufacturers is rare.

In the inspection of memory IC at our company, full inspection under the worst conditions are performed so as to guarantee sufficient operations under all power voltage conditions and timing conditions listed in the data sheet.

An extremely accurate memory tester becomes necessary for performing high-precision inspection with 1ns accuracy. Our company is developing IC memory testers to supply memory ICs with excellent characteristics and quality to users and is establishing the system capable of developing further high-efficiency memory ICs.

1. PROGRAMMING & ERASING OF EPROM

1.1 Programming

Programming to the memory cell of EPROMs is achieved by applying a high voltage to the drain and gate. The high voltage of the drain raises the electron energy of the channel and the voltage of the gate induces the high energy electron (hot electron) injecting to the floating gate. Thus, the charge injected to the floating gate changes the threshold voltage of the memory cell and stores it as the memory information gate changes the threshold voltage of the memory cell and stores it as the memory information. Initially, and after each erasure all bits of EPROMs are in the "1" state.

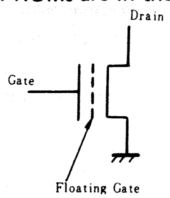


Fig. 1 Equivalent circuit shematic of memory cell

Data can be programmed ("1" → "0") by applying the timing relation waveform and voltage supply stipulated in the specification of EPROMs. Programming can be made to a sequential address and a random address. In addition, writing of only 1 word is also possible. Bits programmed in this manner become "0" in normal power supply condition, however, the output data inverses to "1" when V_{CC} is rises. This voltage (READ V_{CC}) becomes the index for confirming how sufficiently programming has been made to the floating gate. (Of course, the switching speed, input/output levels and others cannot be guaranteed in the range exceeding the power supply condition of V_{CC}.) Fig. 2 shown the correlations among this READ V_{CC}, program pulse width (tpW) and Vpp is designated at 25V ±1V. When Vpp exceeds the maximum rating (including overshoot), the p-n junction of the device sometimes leads to permanent breakage of the element. Taking this point into consideration, please take sufficient care by performing checking of V_{PP} over shoot of the P-ROM writer, etc.

And also take care of negative voltage noise on any pin.

Since a total inspection cannot be performed prior to shipment on matters such as writing & erasing cycles, a guarantee form is not employed but it maintains a standard capable of repeating more than 100 times normally. It can be said to be a sufficient standard when considering the repetition to be about 10 times in maximum in actual use.

Changes on the floating is gradually decreasing and high the temperature is, faster the decreasing rate is. Please refer Fig. 3.

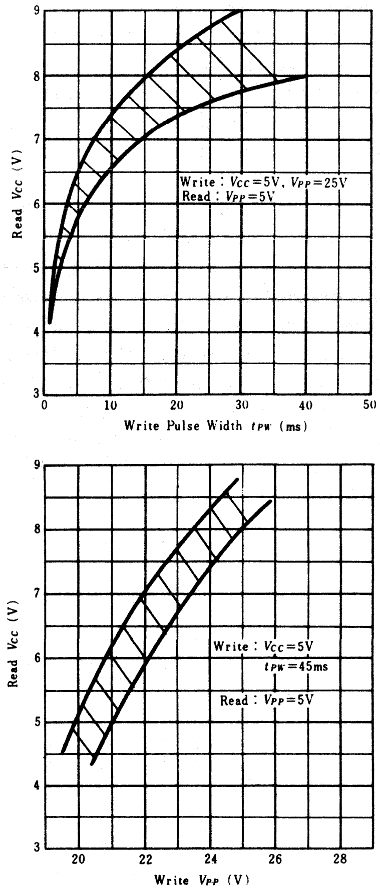


Fig. 2 Typical Programming Characteristics of EPROMs.

1.2 Erasing

Data erasing of EPROMs is performed by the discharge of the electric charge in the floating gate and with the ultraviolet ray irradiation to the memory cell.

The erasing condition is stipulated as ultraviolet ray wavelength 2,537Å and minimum integrated dose 15W. sec/cm^2. This condition can be obtained by placing an ultra violet lamp of 12,000μW/cm^2 within 1 inch of the device and shelving it for about 20 minutes. The material quality of the transparent lid is a sapphire and the transmission ratio of the ultravioletrays is about 70%. However, when contamination and foreign matters exist on the cap surface, the transmission ratio will deteriorate and the time required for erasing will become extended. In such a case, it is necessary to remove the contamination with solvents such as an alcohol, etc., which do not affect the package. Actually, erasing of the element can be sufficiently performed in a shorter time than the stipulated erasing time but since the erasing condition of 15W.sec/cm^2 for performing erasing with a sufficient margin within the device usage condition range has been decided, always be sure to perform irradiation above this condition.

Although the efficiency of ultraviolet rays of a wavelength of less than 3,000 ~ 4,000Å may differ, it has the capability of discharging the electric charge accumulated in the memory cell of EPROMs. The typical erasing characteristics of EPROMs are shown in Fig. 4. The existance of easy-to-erase and hard-to-erase bit in the LSI in this drawing is due to the disperison of accumulated electron volume, etc. Since a slight a mount of ultraviolet rays is contained in fluorescent lights and sunlight, there lies a possibility of causing inversion ("0" → "1") of

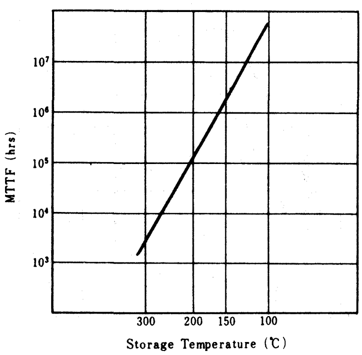


Fig. 3 Typical Data Retention Characteristics

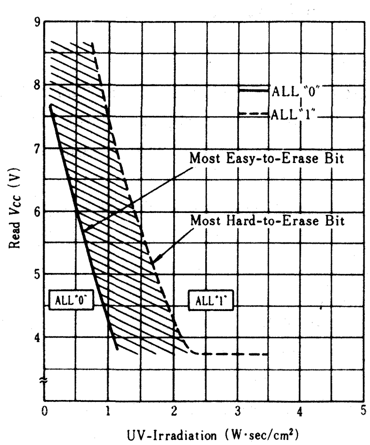


Fig. 4 Typical Erasing Characteristics

the memory information accompanying the vanishing of the charge when such light is irradiated for a long period. Therefore, when there lies a possibility of light being irradiated and a high reliability is demanded, provide measures for shielding the light such as pasting a seal on the lid, etc.

1.3 EPROM Writer

The 16K EPROM wirter stores the program in its internal RAM and writes the program in the EPROM. For this programming, the minimum of 3 functions, the Blank check function prior to programming, the programming function and the Verify function after programming are necessary.

As shown in the drawing, there are also wirters provided with a reverse insertion checking function or pin contact checking function prior to the Blank Check.

The outline of each block is as follows.

(a) Pin contact check

In the connection test of the ROM pin and the socket, normally checking is performed by detecting the forward current of each EPROM pin.

Care is necessary as this forward biased resistance differs according to products of each company.

(b) Reverse insertion check

This check detects the reverse insertion of the device, places the equipment in reset mode and protects the device and equipment.

(c) Blank check

This check is performed prior to programming and checks whether or not it is an erased EPROM or for preventing EPROM reprogramming.

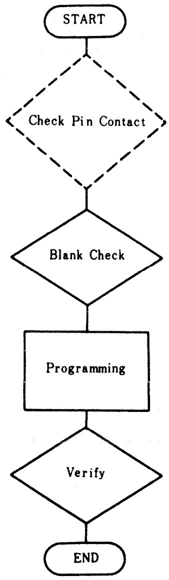
Since the output data in the erased condition are "1" (high level), check whether or not data in EPROM are all "1". It will fail-stop even when 1 bit of "0" (low level).

Normally, it is designed to provide warning with a lamp or buzzer.

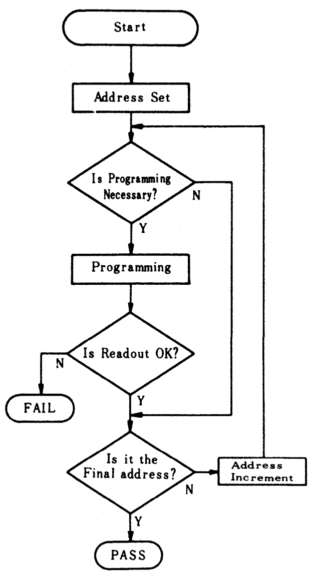
(d) Programming

The function of programming the data in the internal RAM of the writer into EPROM and will fail-stop when programming cannot be made.

The normal flow is as shown below. The EPROM data will be read out prior to programming and compared with the programming data. If they coincide, programming will be skipped and if they differ, programming will be performed. Then, read out will be made again and compared with the programming data, and if they coincide, it will progress to the next address.



(e) Verify
This function is for checking after programming completion whether or not the programming is correct when comparing withthe data in the internal RAM of the writer and it performes fail-stop when it does not coincide. Normally, when it fails, together with lighting of the fail lamp, the address and data are displayed.



(f) How to input the program
There are the following methods for inputing the program data to the internal RAM of the writer.

Normally, paper tape input and teletypewriter input are options.

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitch of the front panel. Used for correction or revision of program
Paper tape input	Read the paper tape furnished from the host system with the tape reader
Teletypewriter input	Input with the teletypewriter. Preparation, correction and list preparation of the program can be made.

1.4 Handling of EPROM

1.4.1 Malfunction caused by static charge

There is a possibility of static charge generation on the glass window of EPROM leading to malfunction of the LSI when the glass surface of EPROM is touched by charged human body or rubbed with plastic or dried cloth. Typical malfunctions are blank fail, write margin fail, etc., which look as if writing has been made in the LSI. This subject has already been mentioned at the international society on LSI reliability and the cause lies in the fact that a charge generates on the chip of LSI due to static charge on the window and this charge remains for a prolonged period.

1.4.2 Regeneration method of charged LSI

When EPROM is accidentally charged and the above-mentioned fail has occurred, the LSI can be completely regenerated to blank condition by irradiating with ultraviolet rays for erasing for a prescribed time. The charge remaining on the chip differs from that accumulated on the floating gate and normally, practically all charges are neutralized when ultraviolet rays of about 50 mW.s/cm^2 are irradiated. Therefore, when static charge fail occurs on EPROM in which the program has been written, it is possible to remove the residual charge on the chip surface without changing the programmed pattern by irradiating ultraviolet rays slightly (about 5 ~ 10 seconds in case of 6.5 mW/cm^2). However, since a slight amount of the charge stored in the floating gate will also be discharged in this case, it is necessary to take are not to apply an "overdose" of ultraviolet rays.

1.4.3 Caution in handling

Since the basic cause is the static charge on the window, its prevention is the most important measure in handling. This is the same as the normal IC electrostatic breakdown measures and the following methods exist.

(1) Earth the operator's body during operation. Do not use gloves, etc., which tend to generate static charge.
(2) Do not rub the glass window with plastic, etc., which are easily cause static charge.
(3) Take care as a slight amount of ion is sometimes contained in the cooling medium spray.
(4) Ultraviolet ray light shielding labels (particularly those containing conductive substances) are also effective from the standpoint of staitc electricity charge prevention.

1.5 Light Shielding Labels

1.5.1 Light shielding effect

In case the data retaining characteristics is essential when EPROM is used in an environment where there is the possibility of exposure to ultraviolet rays, it is effective to paste a light shielding label having an ultraviolet ray absorption effect on the glass window. A special label for this purpose is being marketed, however, those containing metal are generally effective as they absorb ultraviolet rays. 1.4.2 Selection of light shielding label

1.5.2 Selection of light shielding label

In selecting a suitable light shielding label, it is necessary to take care about the following points besides the above-mentioned items.

(1) Adhesive property (Mechanical strength)

Care is necessary in case of reusing the label or adherence of dust as the bonding force is weakened.

Besides, when peeling off, the label may induce static charges that before using EPROMs, erasing-reprogramming or short time erasure will be recommended.

(2) Permissible temperature range

Labels have their own maximum ratings and the range of guarantee, as well as their degradation characteristics. Please check them before using them.

(3) Moistureproofness

Upon considering the above points, it is necessary to make suitable selection according to the usage purpose.

2. PROGRAMMING OF BIPOLAR PROMS

2.1 Programming System

The storing system of the Bipolar PROM can be generally classified into 2 systems; the Blown diode system and fuse system.

The latter is a system in which the metal-made fuse is burned off by current (Fig. 5). In the former, Emitter-Base junction is short-circuited by Al, which has penetrated into Base because of current pulse applied to E-B junction (Fig. 6). Generally, the blown diode type is considered to be more reliable. A grow back phenomenon, that is, migration and recombination of the metal, is seen in fuse system. HITACHI devices use the blowin diode system.

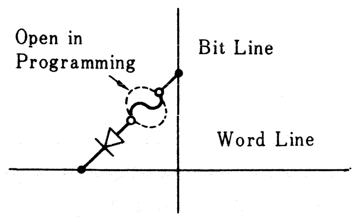


Fig. 5 Fuse system

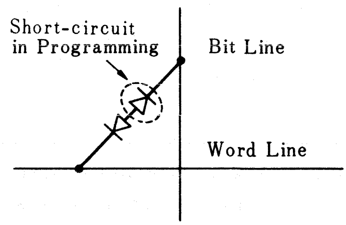


Fig. 6 Blown diode system

2.2 Programming Method

Programming is executed by the conventional programming equipment (PROM writer) using a board suited to the product.

First, check if all bits are programmable (Blank check), next write the pattern you want to program one by one bit. At every application of current pulse, confirm that program is available by sensing output level. And when programming has been completed, apply additional pulse. This process should be performed for all bits into which you want to write, and as you have completed programming, check (Verify) if you have programmed in the same pattern as you intended. If you do not find any mistake, programming has been completed.

For Blank check, Sense and Verify whether output pin level is high (non-programmed) or low (programmed) is checked by sense current (Is). Vs – Is characteristic of normal series and S series is shown in Fig. 8 and 9, respectively. Specified value of sense current (Is) of both normal series and S series is 20 mA, and voltage reference level is 7.5 V.

Fig. 10 and 11 show the relation between program current and program pulse number necessary for 1 bit to be written. With consideration of its influence on breakdown voltage, program current is specified as 130 mA in normal series and as 90 mA in S series.

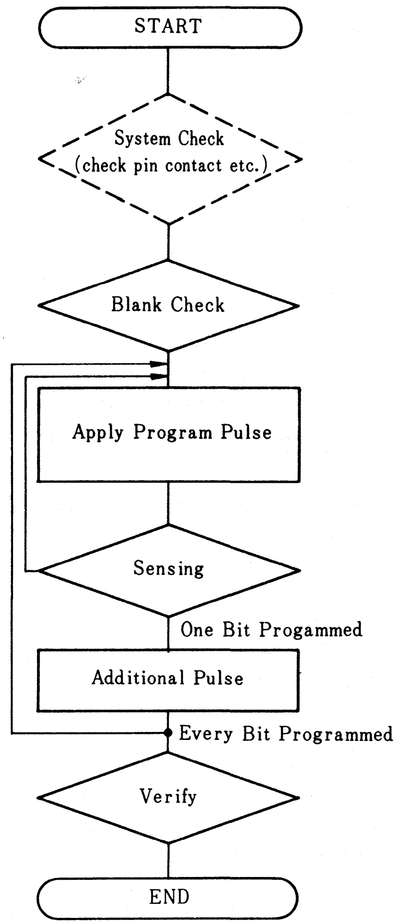


Fig. 7 Programming Flow of PROM

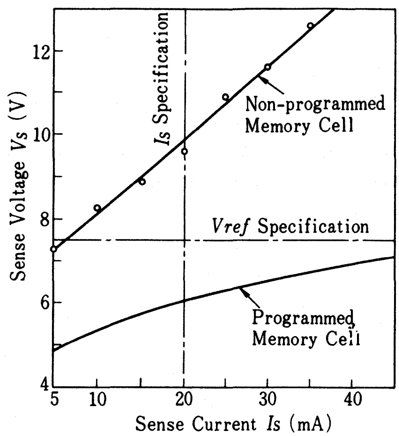


Fig. 8 Vs — Is Characteristic of Normal Series (HN25089)

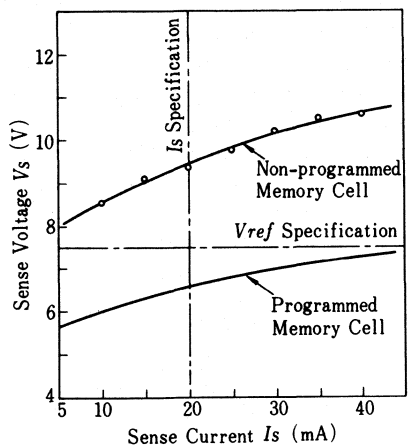


Fig. 9 Vs — Is Characteristic of S Series (HN25169S)

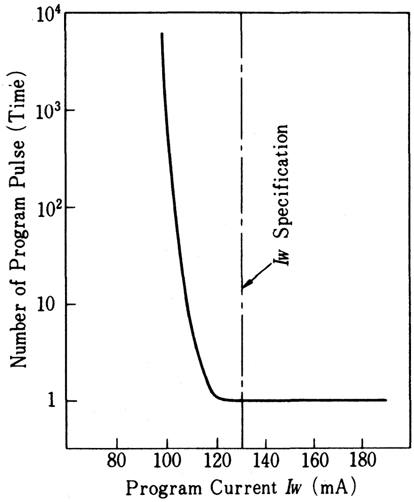


Fig. 10 Program Pulse — Iw Characteristic of Normal Series (HN25089)

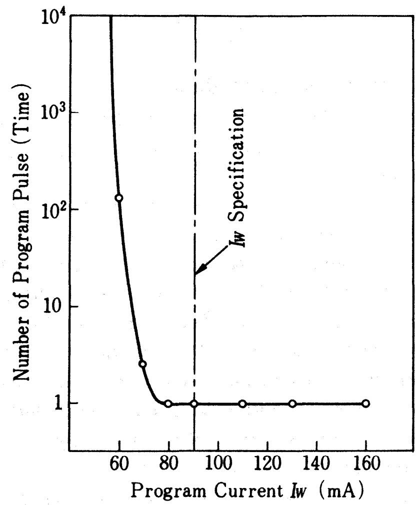


Fig. 11 Program Pulse — Iw Characteristic of S Series (HN25169S)

2.3 Programming Characteristics of Hitachi Bipolar PROM

- Small program current

130 mA for normal series, and 90 mA for S series are required for programming. Therefore, there are few bad effects caused by breakdown voltage degradation and parasitic effects.

- Fast programming speed

As seen in Fig. 10 and 11, program pulse for 1 bit memory cell can be mostly written at one time. Consequently, the program time per device is quite short. In case of 8K bit, for example, only 2 or 3 seconds at an average are required.

- High programming yield

Unlike the MOS PROM, the Bipolar PROM cannot be rewritten, once it is written into the memory cell.

Therefore, it does not allow programming and inspection of the product prior to delivery. Due to this, sometimes a defective product (which does not allow programming) might be delivered.

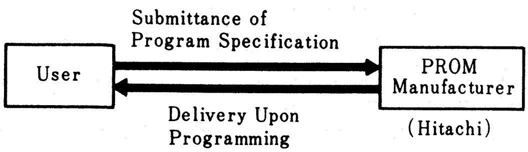
Generally, the programming efficiency percentage is 90~95% when programming is performed on the user's side. Special tests such as actually performing programming on the dummy cell in the chip, performing continuity test of all memory cells, etc., are made prior to delivery for minimizing the possiblity to deliver defective products.

2.4 Programming

There are two methods in the programming of PROM. That is, the method when programming is made by PROM manufacturer and delivered and the method when programming is made on the user's side. Both these methods and procedures will be explained below.

2.4.1 Programming performed by the PROM manufacturer

As shown in the drawing below, the manufacturer receives the program specification (specification designating the program pattern) from the user, performs writing (Programming) in accordance with the specification and performs delivery. In this case, a special writing fee is charged.



2.4.2 Programming performed by user

In this case, the following three items must be prepared by the user.

1 PROM WRITER (Main unit of programming equipment)
  One capable of being used in common with equivalent products of other companies.
2 Performance board (Exclusive board designated by each manufacturer)
  Minimum of 1 board for Hitachi PROM.
3 Sockets (sockets suited to product)
  Minimum of one socket per product. These sockets are purchased from the PROM WRITER manufacturer.

The relationship among PROM WRITER manufacturer, Hitachi and user is shown in Fig. 12.

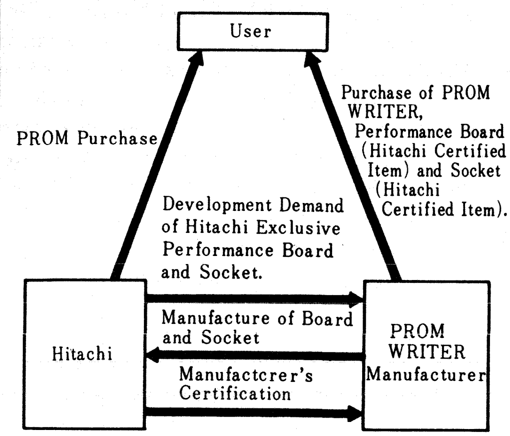


Fig. 12 Relationship among Hitachi, User and PROM WRITER manufacturer

As indicated above, the user purchases the performance board and sockets exclusively for Hitachi products together with purchasing the PROM WRITER.

2.5 Programming Device

There are about ten programming device manufacturers. However, this does not mean that any manufacturer's device will suffice. The reasons are as follows.

- It costs several hundreds of thousands or several million yen to have a programming device manufacturer develop a dedicated board for Hitachi and to qualify it.
- The suitability of the programming device affects the programming efficiency. Therefore, it should be a device of a reliable manufacturer.
- The servicing setup for handling troubles should be consolidated. The setup should be one that judgement can be accurately made on whether it is a writing device trouble or PROM trouble.

Hitachi has prepared a list of recommended manufacturers which meet the above requirements. Please contact our sales engineering staff for information in this regard.

The writing of the custom program code into the mask ROM is performed by the CAD system using a large-sized computer. You should submit the data of the ROM code in conformity with the specification explained below by either paper tape, EPROM or magnetic tape. In addition, enter your instructions such as the chip select, customer part number, etc., in the "ROM Specification Identification Sheet" and attach it to the ROM code data.

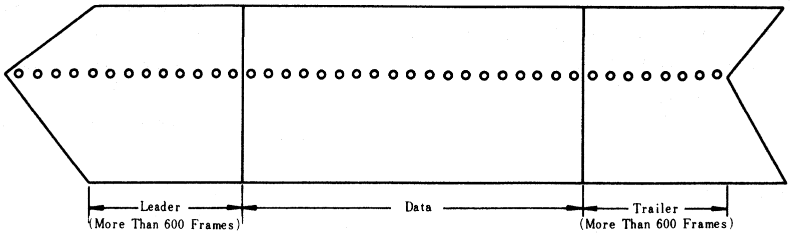
1. Overall Specification

Since the submitted paper tape, card or magnetic tape is fed into the large-size computer as it is, observe the following specifications.

1.1 Specification of Paper Tape

1.1.1 Any color paper tape may be used as long as it is a marketed 1 inch wide paper tape for computers. However, a black color paper tape is recommended.

1.1.2 Take more than 600 frames for the leader and trailer.



1.1.3 Parity mode

The presence and type of parity are clearly described in the "ROM Specification Identification Sheet".

There are following modes in the parity system.

(1) With parity

Even parity .... EVEN

Odd parity .... ODD

(2) Without parity

1.1.4 Use the 8 unit ASC11 code as the code.

1.2 Specification of Magnetic Tape

1.2.1 Use the following type of magnetic tape which can be netered in a magnetic tape device which is compatible with the IBM magnetic tape device.

(1) Length .... 2,400 feet, 1,200 feet or 600 ffet

(2) Width .... 1/2 inch

(3) Channel .... 9 channels

(4) Bit density .... 800 BPI or 1,600BPI (Clearly state which it is in the "ROM Specification Indentification Sheet".)

1.2.2 Use the EBCDIC code as the use code.

1.2.3 Make the format of the magnetic tape as described below.

(1) No leading tape mark

(2) No label

(3) Record size .... 80 byte/1 record

(4) Block size .... 10 records/1 block

(5) The end of the file should be indicated by 2 successive tape marks (TM).

1.2.4 Ensure that the magnetic tape becomes of 1 roll for each chip. Since extending the single-chip portion over several rools is impermissible, submit by compiling into the single-chip portion for each roll.

2. Data Mode

2.1 HMCS6800 Load Module Mode

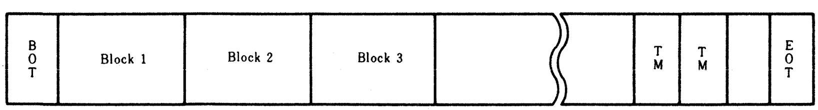
This mode is the object mode output from the assembler of HMCS6800.

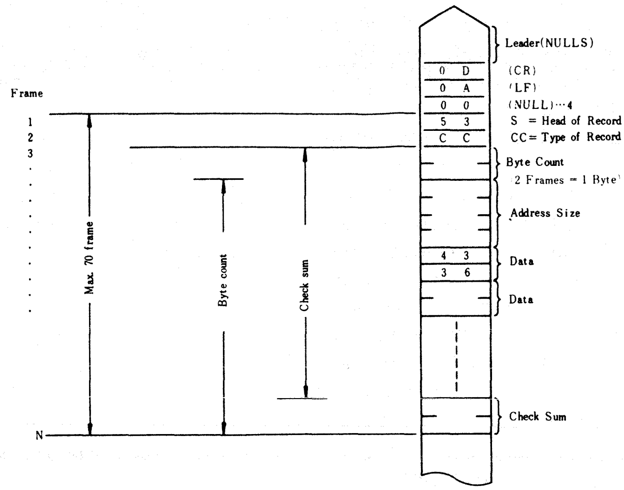
2.1.1 Divide the 8 bit code into the upper and lower 4 bit codes and convert each into hexadecimal notation.

(Example) The code of 1100 0110 becomes as follows under binary notation.

(Upper 4 bits)	(Lower 4 bits)	
D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0	Bit weight (ROM output equivalence)
1 1 0 0	0 1 1 0	

2.1.2 The composition of the load module mode is shown below by taking the case of paper tape as the example. The numbers written in the tape are ASCII code hexadecimal numbers of the data.





(Note) The check sum is a technique which disregards the complement on one of each bit sum of the 8 bits.

2.1.3 The actual load module mode becomes as shown below.

Frame		CC=30 Header record		CC=31 Data record		CC=39 End of file record	
1	Record Start	5 3	S	5 3	S	5 3	S
2	Record Type	3 0	0	3 1	1	3 9	9
3 4	Byte Count	3 0 3 6	0 6	3 1 3 6	1 6	3 0 3 3	0 3
5 6 7 8	Address Size	3 0 3 0 3 0 3 0	0000	3 1 3 1 3 0 3 0	1100	3 0 3 0 3 0 3 0	0000
9 10	Data	3 4 3 8	48-H	3 9 3 8	9 8	4 6 4 3	FC (Check Sum)
	Data	3 4 3 4	44-D	3 0 3 2	0 2		
	Data	3 5 3 2	52-R				
N	Check Sum	3 1 4 2	1B (Check Sum)	4 1 3 8	A8 (Check Sum)		

S0 indicates the head of the file and S9 indicates the end of the file. The actual data enters following S1. It means that the data starts from the address (hexadecimal) indicated in the address size. The address of the address size of the data recorder is compared with the next data recorder address by counting in increments of 1 byte of the data and checking whether it is sequential or not. In places where the address is skipped, the data of 00 or FF enters hexadecimally. The printed example of the paper tape of the HMCS6800 load module mode is as shown below.

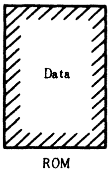
Example

```
Header Record  →S00B00005820455841 4D504CB5
Data Record    →S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24
Data Record    →S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06
End of
File Record    →S9030000FC
```

2.1.4 The ROM code data are capable of handling the following 4 types of cases. A header recorder is required in front of the data recorder and an end of file recorder at the back of the data recorder.

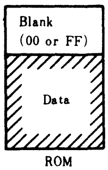
(1) Case when the data reaches full capacity of ROM

The ROM recorder for 1 chip enters into the data recorder. Since the address of the address size of the data recorder counts the data and checks whether or not it is in a sequential address, it becomes necessary that the address not be skipped. The ROM head address column of the "ROM Specification Identification Sheet" becomes 0.

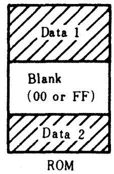


(2) Case when data is input from en route of ROM

In this case, perform entry by decimal notation in the ROM head address column of the "ROM Specification Identification Sheet" on which ROM address you wish to input the data. The data 00 or FF will enter into the blank address by hexadecimal notation.

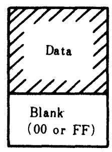


(3) Case when data is input by skipping intermediate address



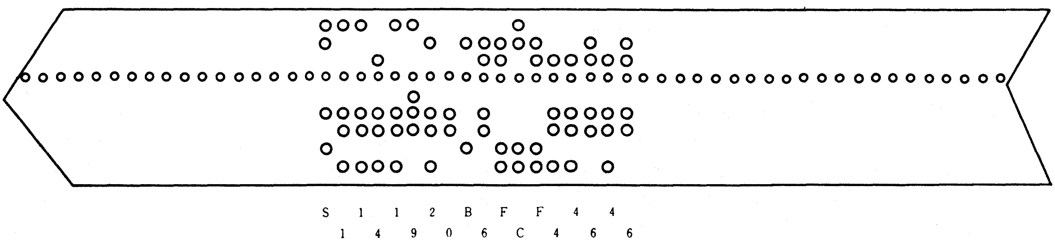
The address of the address size of the data recorder is counted in increments of 1 byte of the data, compared with the next address of the data recorder and checked whether or not it is sequential. The data 00 automatically enters by hexadecimal notation into the ROM code of the skipped address. Therefore, the writing of data as in the following drawing is also possible. In this case, perform entry into the "ROM Specification Identification Sheet" that the ROM head address enters from 0 address for data I and from which address it enters for data II.

(4) Case when the data is less than the full capacity of ROM



In case the data volume is less than the total byte capacity of ROM LSI when the end of file recorder appears, it becomes written as the ROM code as shown in the following drawing.

(Example) Indicates the example of the paper tape when the data recorder is S1141920B6-FC ...



2.2 BNPF Mode

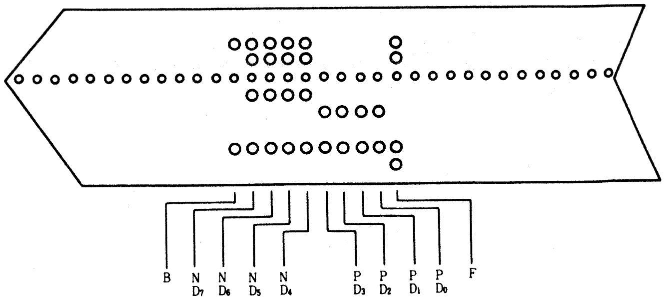
2.2.1 One word is symbolized by the word start mark B, the bit content represented by 8 characters of P and N, and the BNPF slice composed of successive 10 characters of the work end mark F.

2.2.2 The contents from F of one BNPF slice up to B of the next BNPF slice are ignored.

(Example) The code of 0F by hexadecimal notation is symbolized as shown below (in case of paper tape)

2.2.3 It is necessary to designate the bit pattern (BNPF slice) on all ROM addresses. Therefore, the term of the ROM head address of "ROM Specification Identification Sheet" always becomes 0.

B .... Indicates start of 1 word.
N .... Indicates "0" of 1 bit data.
P .... Indicates "1" of 1 bit data.
F .... Indicates end or 1 word.

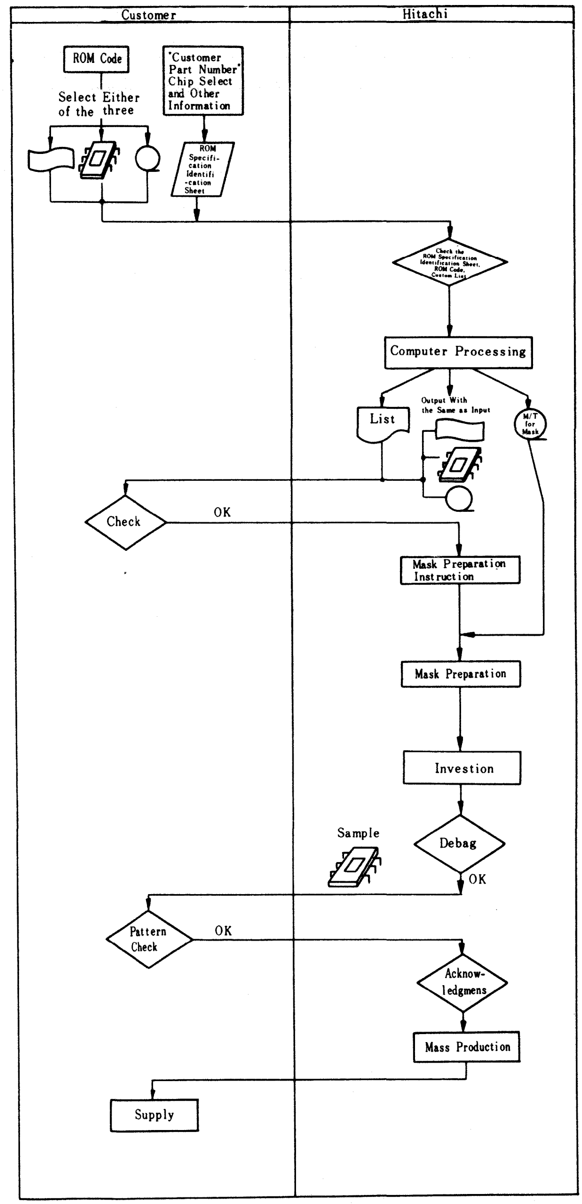


Note 1) Sometimes X is used besides P and N in the display of the word content by the BNPF slice.
X means that the user is not concerned whether the bit is P or N. However, since it is necessary to decide the P or N for performing tests, Hitachi performs selection of P or N. The results are informed by making entry in the identification table.

Note 2) The contents of the BNPF slice are not only those with the continuation of PN and the form of B*nF can also be used. This means that the content of the slice existing just prior to this word will be repeated for n words from this word.
For example, when B*4F exists at the 10th word, it means that the content of the 9th word will be repeated in the 10th, 11th, 12th and 13th words. (However, it does not necessarily follow that the X content of Note 1 above will be repeated.) n shall start from 1 and be a number below the total addresses of ROM.

Note 3) When a certain block is not used (when an unused ROM address exists), disposition can be made by utilizing Notes 1 and 2.

Mask ROM Development Flowchart



DATA SHEETS

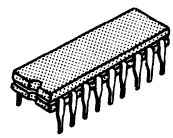
MOS STATIC RAM

HM472114A-1, HM472114A-2
HM472114AP-1, HM472114AP-2

1024-word×4-bit Static Random Access Memory

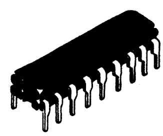
- Fast Access Time .... HM472114A-1 150ns (max.)
  HM472114A-2 200ns (max.)
- Low Operating Power .... 200mW (typ.)
- Single +5V Supply
- Completely Static Memory .... No Clock or Refresh Required
- Fully TTL Compatible .... All Inputs and Outp
- Common Data Input and Output Using Three-state Outputs
- N-channel Si Gate MOS Technology
- Pin Equivalent with Intel 2114L Series

HM472114A-1, HM472114A-2



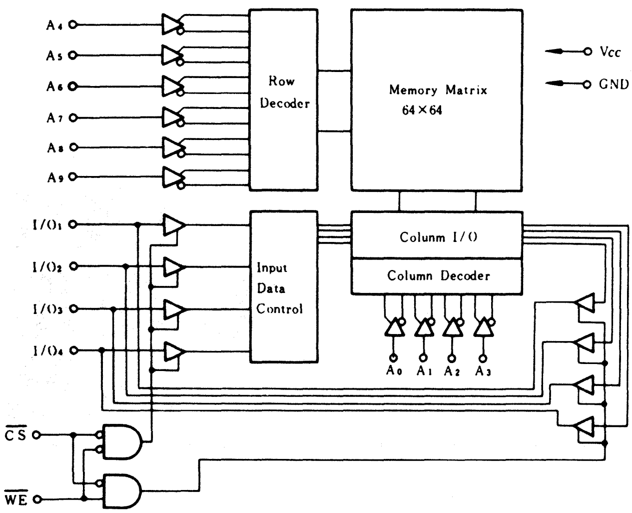
(DG-18)

HM472114AP-1, HM472114AP-2

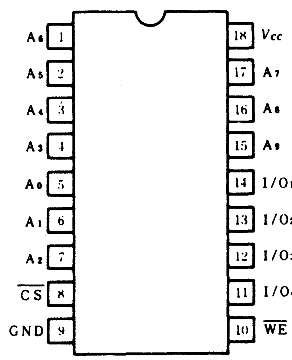


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage*	V_T	−0.5 to +7	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	℃
Storage Temperature (Plastic)	T_{stg}	−55 to +125	℃

* In respect to GND.

■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.5	—	0.8	V
	V_{IH}	2.0	—	V_{CC}+1.0	V
Operating Temperature	T_{opr}	0	—	70	℃

■DC AND OPERATING ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in}=0~5.5V	—	—	10	μA
I/O Leakage Current	$\lvert I_{LO}\rvert$	$\overline{CS}$=2.0V, $V_{I/O}$=0.4V~V_{CC}	—	—	10	μA
Supply Current	I_{CC}	V_{in}=5.5V, $I_{I/O}$=0mA	—	35	60*	mA
Input Voltage	V_{IL}		−0.5	—	0.8	V
	V_{IH}		2.0	—	V_{CC}+1.0	V
Output Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
	V_{OH}	I_{OH}=−0.6mA(V_{CC}=4.5V)	2.4	—	—	V
		I_{OH}=−1.0mA(V_{CC}=4.75V)	2.4	—	—	

Note) * : in respect to HM472114A/AP-2. This value of HM472114A/AP-1 is 70mA.

■CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	5	7	pF

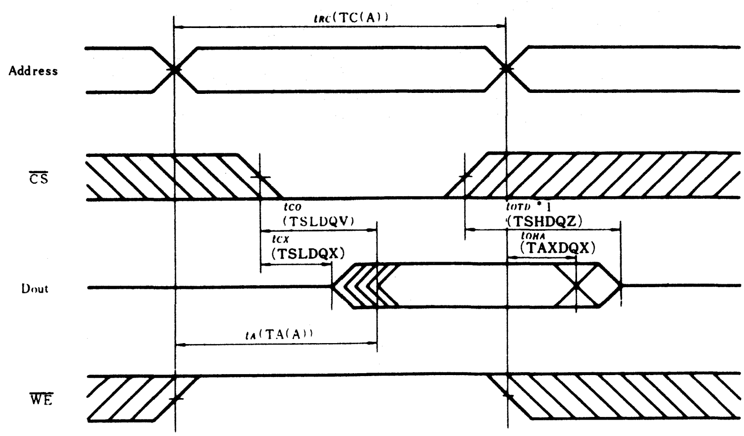
■AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

● AC TEST CONDITIONS

Input Level 2.4V, 0.8V
Input Rise and Fall Time 10ns
Timing Measurement Level 1.5V
Output Load .... 1 TTL + 100pF

● READ CYCLE

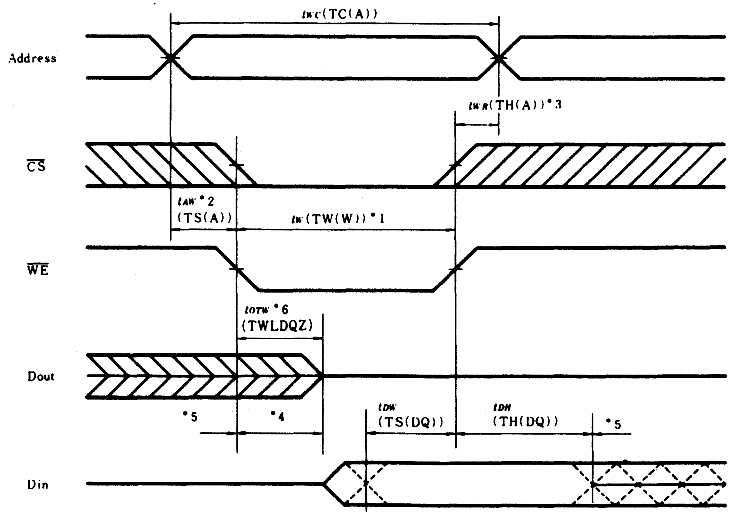
Item	Symbol	HM472114A-1		HM472114A-2		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Access Time	t_A	—	150	—	200	ns
$\overline{CS}$ to Output Valid	t_{CO}	—	70	—	70	ns
$\overline{CS}$ to Output Active	t_{CX}	10	—	10	—	ns
Output 3-state from Deselection	t_{OTD}	—	60	—	60	ns
Output Hold from Address Change	t_{OHA}	20	—	50	—	ns



NOTE: 1) t_{OTD} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

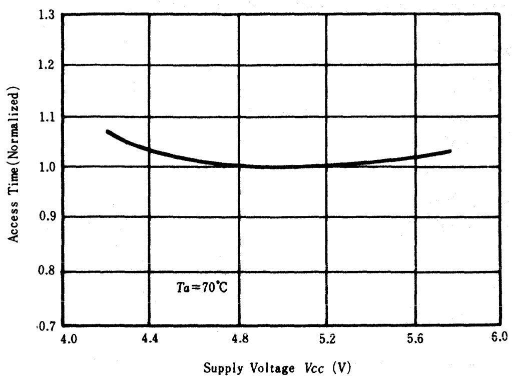
● WRITE CYCLE

Item	Symbol	HM472114A-1		HM472114A-2		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Address to Write Setup Time	t_{AW}	20	—	20	—	ns
Write Pulse Width	t_W	120	—	120	—	ns
Write Release Time	t_{WR}	0	—	0	—	ns
Output 3-state from Write	t_{OTW}	—	60	—	60	ns
Data to Write Time Overlap	t_{DW}	70	—	120	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns

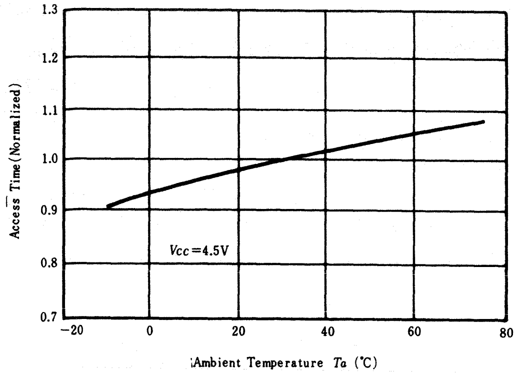


NOTE:
1) A WRITE state occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$ (t_W).
2) t_{AW} is measured from the address setting to the latter of $\overline{CS}$ or $\overline{WE}$ going low.
3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4) During this period I/O pins are in the output state, the input signals of opposite phase to the outputs must not be applied to them.
5) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the input signals of opposite phase to the outputs must not be applied to them.
6) t_{OTW} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

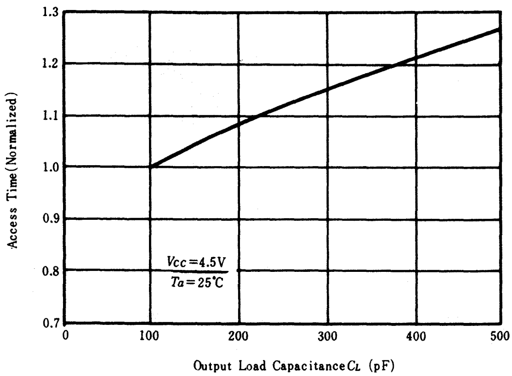
ACCESS TIME vs. SUPPLY VOLTAGE



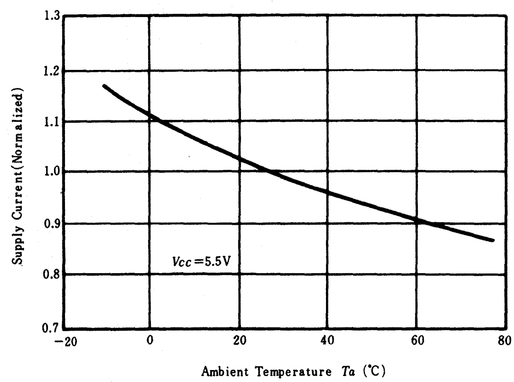
ACCESS TIME vs. AMBIENT TEMPERATURE



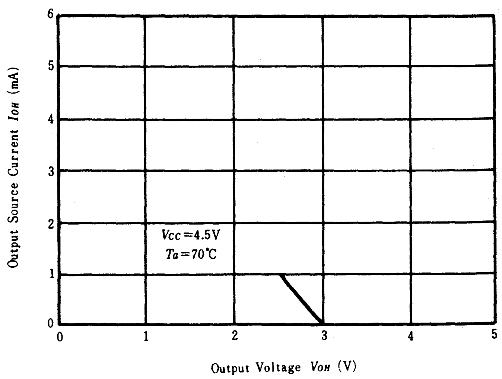
ACCESS TIME vs. OUTPUT LOAD CAPACITANCE



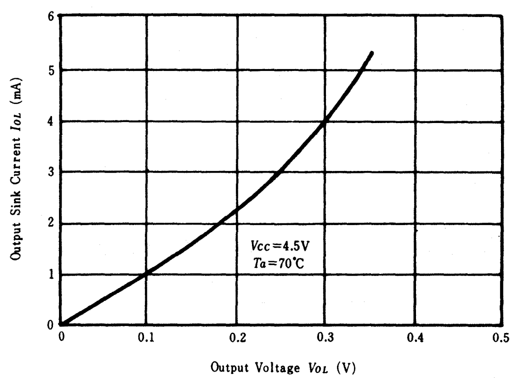
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

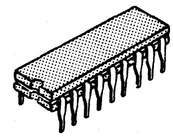


HM472114-3, HM472114-4
HM472114P-3, HM472114P-4

1024-word×4-bit Static Random Access Memory

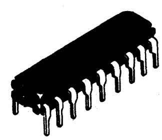
- Access Time .... HM472114-3 300ns (max.)
  HM472114-4 450ns (max.)
- Low Operating Power .... 200mW (typ.)
- Single +5V Supply Voltage
- Completely Static Memory .... No Clock of Refresh Required
- Directly TTL Compatible .... All Inputs and Outputs
- Common Data Inputs and Output
- Three-state Outputs
- DC Standby Mode .... Reduces V_{CC}
- N-channel Si Gate MOS Technology
- Interchangeable with Intel 2114L Series

HM472114-3, HM472114-4



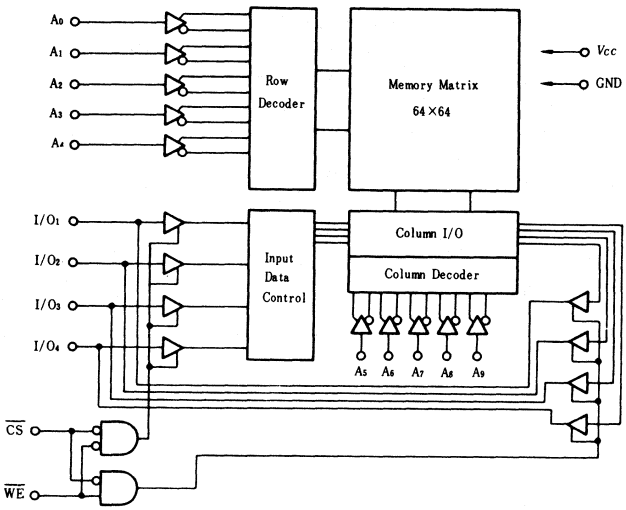
(DG-18)

HM472114P-3, HM472114P-4

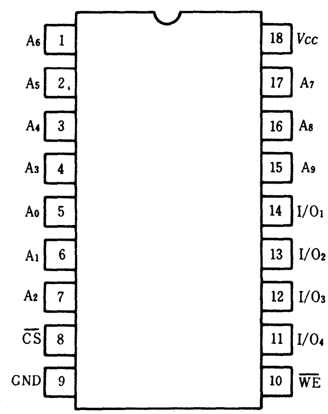


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage	V_T	−0.5 to +7	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C

■RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.5	—	0.8	V
	V_{IH}	2.0	—	V_{CC}+1.0	V
Operating Temperature	T_{opr}	0	—	70	°C

■DC AND OPERATING ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0～+70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in}=0～5.5V	—	—	10	μA
I/O Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=2.0V, $V_{I/O}$=0.4～V_{CC}	—	—	10	μA
Supply Current	I_{CC}	V_{in}=5.5V, $I_{I/O}$=0mA	—	35	60	mA
Input Voltage	V_{IL}		−0.5	—	0.8	V
	V_{IH}		2.0	—	V_{CC}+1.0	V
Output Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
	V_{OH}	I_{OH}=−0.6mA, V_{CC}=4.5V	2.4	—	—	V
		I_{OH}=−1.0mA, V_{CC}=4.75V	2.4	—	—	

■CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	5	10	pF

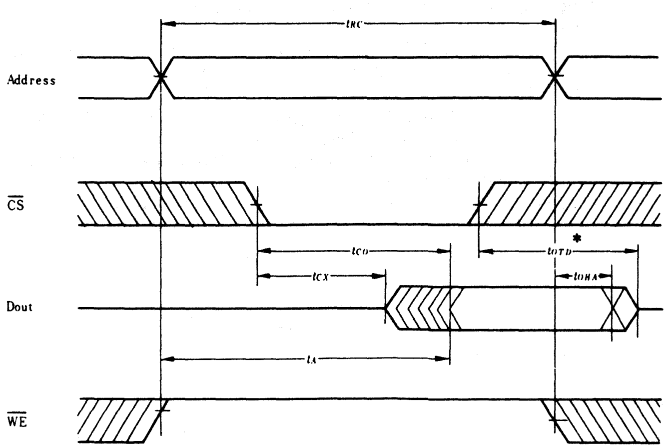
■AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

● AC TEST CONDITIONS

Input Level 2.4V, 0.8V
Input Rise and Fall Time 10ns
Timing Measurement Level 1.5V
Output Load .... 1 TTL and 100pF

● READ CYCLE

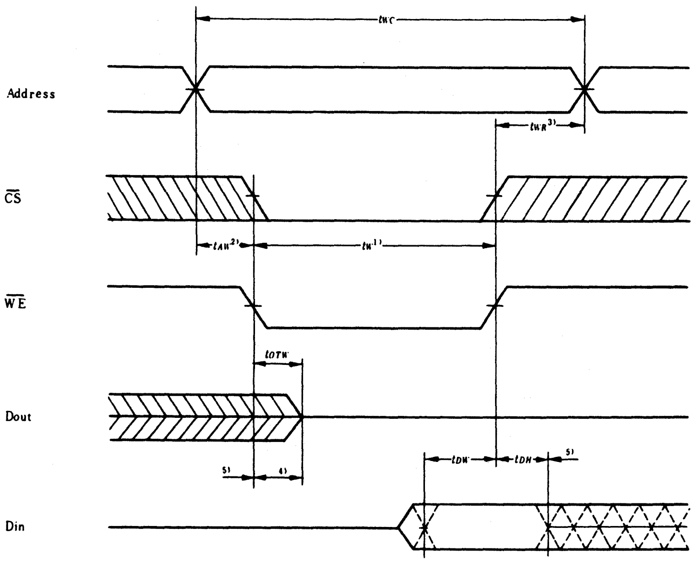
Item	Symbol	HM472114-3, HM472114P-3		HM472114-4, HM472114P-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	300	—	450	—	ns
Access Time	t_A	—	300	—	450	ns
$\overline{CS}$ to Output Valid	t_{CO}	—	100	—	120	ns
$\overline{CS}$ to Output Active	t_{CX}	20	—	20	—	ns
Output 3-state from Deselection	t_{OTD}	—	80	—	100	ns
Output Hold from Address Change	t_{OHA}	50	—	50	—	ns



NOTE: 1) t_{OTD} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

■WRITE CYCLE

Item	Symbol	HM472114-3, HM472114P-3		HM472114-4, HM472114P-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	300	—	450	—	ns
Address to Write Setup Time	t_{AW}	20	—	50	—	ns
Write Pulse Width	t_W	150	—	200	—	ns
Write Release Time	t_{WR}	0	—	0	—	ns
Output 3-state from Write	t_{OTW}	—	80	—	100	ns
Data to Write Time Overlap	t_{DW}	150	—	200	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns



Notes: 1) Both $\overline{CS}$ and $\overline{WE}$ are paced in the WRITE state during low level period (t_W).
2) t_{AW} is an interval from the address setting through the catter of $\overline{CS}$ or $\overline{WE}$ going low.
3) t_{WR} is from the earlier rise pulse of $\overline{CS}$ or $\overline{WE}$ till the end of the write cycle (t_{WC}).
4) During this period the pulse is output state so that the input signal which is the opposit phase to the output must not be applied to the I/O terminal.
5) During this period, when the $\overline{CS}$ signal is at low level, the pulse is output so that the input signal which is the same in phase with the output data may be applied, if required. Do not however apply the input signal of reverse phase.
6) t_{OTW} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

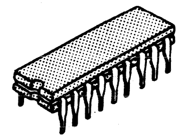
HM4334-3, HM4334-4
HM4334P-3, HM4334P-4

1024-word × 4-bit Static CMOS RAM

■FEATURES

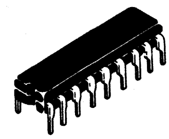
- Single 5V Supply
- Low Power Standby and Low Power Operation; Standby: 10μW (typ.) Operation: 20mW (typ.)
- Access Time; HM4334/P-3: 300 ns (max.) (5V±5%) HM4334/P-4: 450 ns (max.) (5V±10%)
- Directly TTL Compatible: All inputs and outputs
- Common Data Input and Output using Three-state Outputs
- On Chip Address Register

HM4334-3, HM4334-4



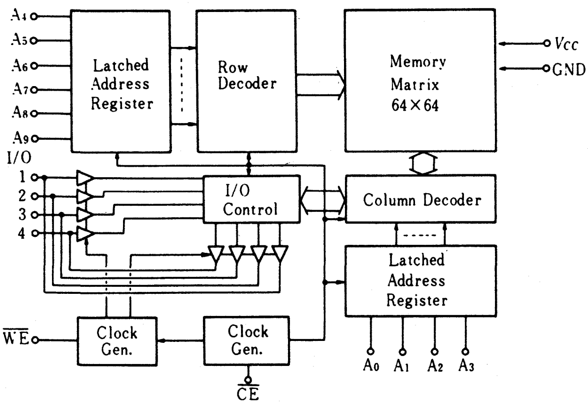
(DG-18)

HM4334P-3, HM4334P-4

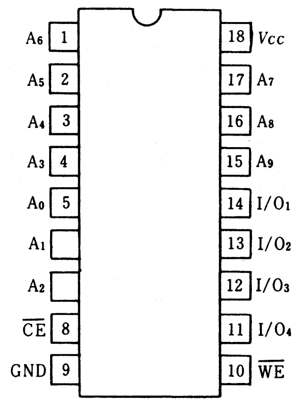


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin*	V_T	−0.3 to V_{CC} +0.5	V
Power Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Cerdip)	T_{stg}	−65 to +150	°C

* with respect to GND

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	HM4334/P-3			HM4334/P-4			Unit
		min	typ	max	min	typ	max	
Supply Voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
	GND	0	0	0	0	0	0	V
Input Voltage	V_{IH}	2.4	—	V_{CC}+0.5	2.4	—	V_{CC}+0.5	V
	V_{IL}	−0.3	—	0.8	−0.3	—	0.8	V

■DC AND OPERATING CHARACTERISTICS

(Ta=0 to +70°C, GND=0V, HM4334/P-3 : V_{CC}=5V±5%, HM4334/P-4 : V_{CC}=5V±10%)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	−1.0	—	+1.0	μA
Output Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, V_{out}=0 to V_{CC}	−1.0	—	+1.0	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE}$=0V, $V_{IN}=V_{CC}$, $I_{I/O}$=0	—	—	1.0	mA
	I_{CC2}	$\overline{CE}$=0.8V, V_{IN}=2.4V, $I_{I/O}$=0	—	2.5	5.0	mA
Average Operating Current	I_{CC3}	V_{IN}=0 or V_{CC}, f=1MHz, duty 50%, $I_{I/O}$=0	—	4	7	mA
Standby Power Supply Current	I_{CCL}	$\overline{CE} \geq V_{CC}-0.2V$	—	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.0mA	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

■CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Condition	min	typ	max	Unit
I/O Terminal Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	10	pF
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF

■AC CHARACTERISTICS

(Ta=0 to +70°C, GND=0V, HM4334/P-3 : V_{CC}=5V±5%, HM4334/P-4 : V_{CC}=5V±10%)

Item	Symbol		HM4334/P-3			HM4334/P-4			Unit
			min	typ	max	min	typ	max	
Read or Write Cycle Time*	TELEL	t_C	460	—	—	640	—	—	ns
Chip.Enable Access Time	TELQV	t_{AC}	—	—	300	—	—	450	ns
Chip Enable to Output Active	TELQX	t_{CX}	50	—	—	50	—	—	ns
Output 3-state from Deselection	TEHQZ	t_{OFF1}	—	—	100	—	—	100	ns
Write Enable Output Disable Time	TWLQZ	t_{OFF2}	—	—	100	—	—	100	ns
Chip Enable Pulse Width**	TELEH	t_{CE}	300	—	—	450	—	—	ns
Chip Enable Precharge Time	TEHEL	t_P	120	—	—	150	—	—	ns
Address Hold Time	TELAX	t_{AH}	100	—	—	100	—	—	ns
Address Setup Time	TAVEL	t_{AS}	20	—	—	20	—	—	ns
Read Setup Time	TWHEL	t_{RS}	0	—	—	0	—	—	ns
Read Hold Time	TEHWL	t_{RH}	0	—	—	0	—	—	ns
Write Enable Setup Time	TWLEL	t_{WS}	−20	—	—	−20	—	—	ns
$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	TWLEH	t_{WPL}	300	—	—	450	—	—	ns
Chip Enable to Write Enable Delay Time	TELWL	t_{CWD}	300	—	—	450	—	—	ns
Write Enable Hold Time	TEHWH	t_{EWH}	0	—	—	0	—	—	ns
Write Hold Time	TELWH	t_{WH}	300	—	—	450	—	—	ns
Data Input Setup Time	TDVWH TDVEH	t_{DS}	200	—	—	350	—	—	ns
Data Hold Time	TWHDX TEHDX	t_{DH}	0	—	—	0	—	—	ns
Write Data Delay Time	TWLDV	t_{WDS}	100	—	—	100	—	—	ns
Chip Enable Rise/Fall Time	TT	t_T	—	—	300	—	—	300	ns

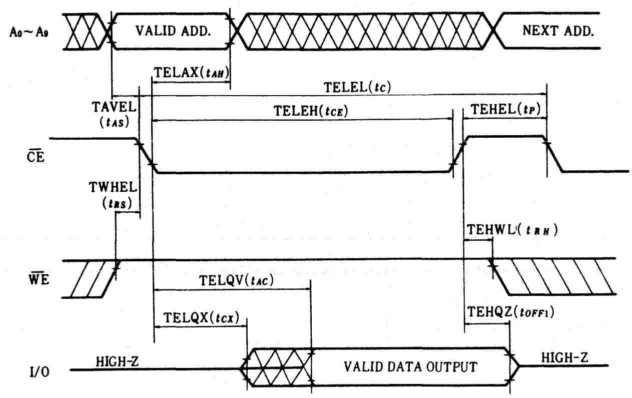
* TELEL(t_C)=TELEH(t_{CE})+TEHEL(t_P)+t_r(20ns)+t_f(20ns)

** For Read Modify Write Cycle, TELEH(t_{CE})=TELWL(t_{CWD})+TWLEH(t_{WPL})+t_f(20ns)

■AC TEST CONDITIONS

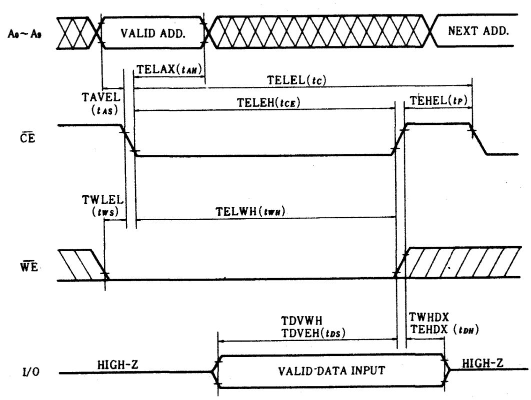
Input Level	2.4V, 0.8V
Input Rise and Fall Time	20ns
Timing Measurement Level	2.4V, 0.8V
Reference Level	V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load	1 TTL and C_L = 100 pF

● READ CYCLE



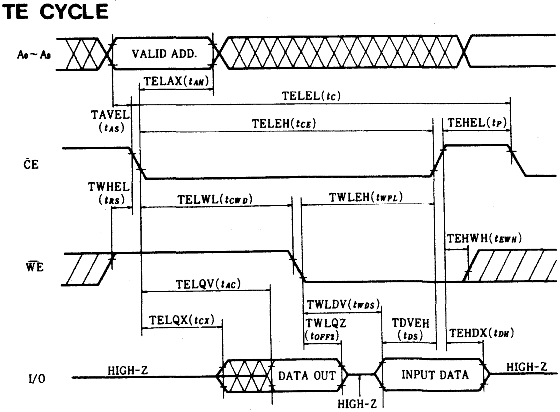
Note) *; TEHQZ (t_{OFF_1}) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

● WRITE CYCLE



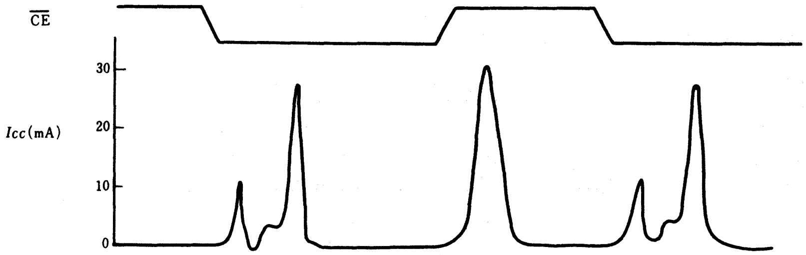
Note) t_{DS} and t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

● READ MODIFY WRITE CYCLE



*; TWLQZ (t_{OFF_2}) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

● CURRENT WAVEFORM



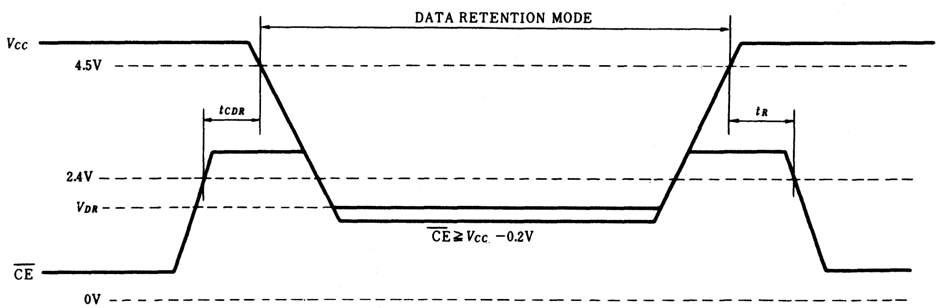
[NOTE] V_{CC} = 5.0V, T_a = 25°C

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

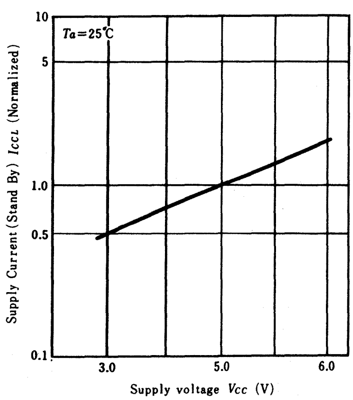
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Power Supply Current	I_{CCDR}	V_{DR}=3.0V	—	0.5	50	μA
Chip Deselection to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*	—	—	ns

* t_{RC}=Read Cycle Time

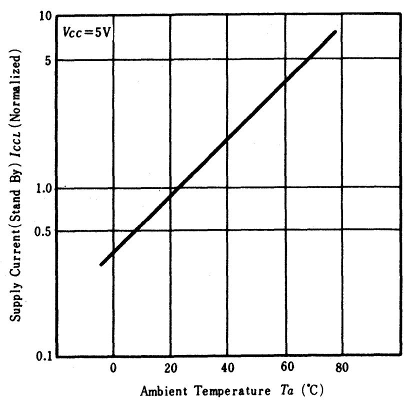
● LOW V_{CC} DATA RETENTION TIMING



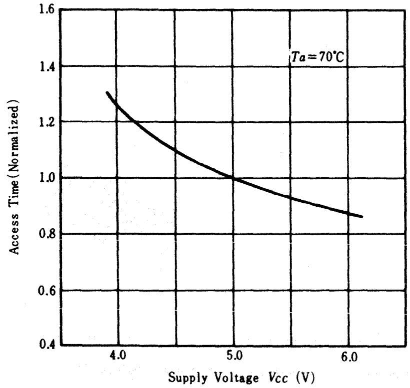
SUPPLY CURRENT vs. SUPPLY VOLTAGE



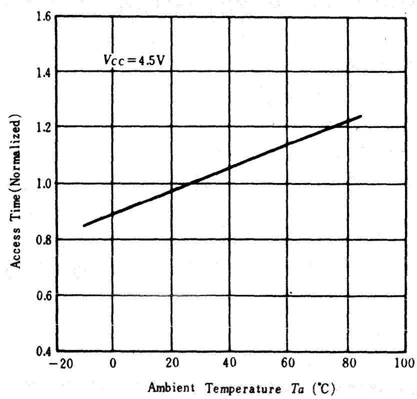
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



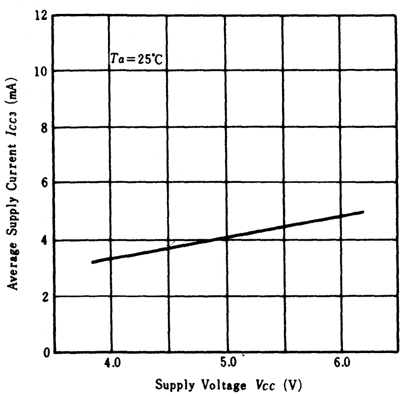
ACCESS TIME vs. SUPPLY VOLTAGE



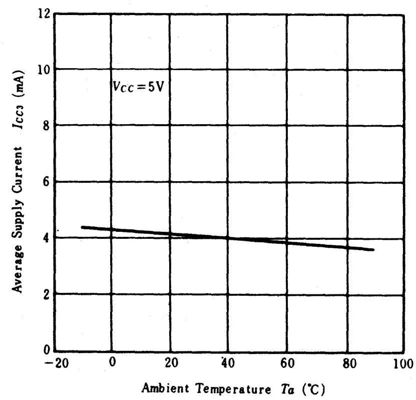
ACCESS TIME vs. AMBIENT TEMPERATURE



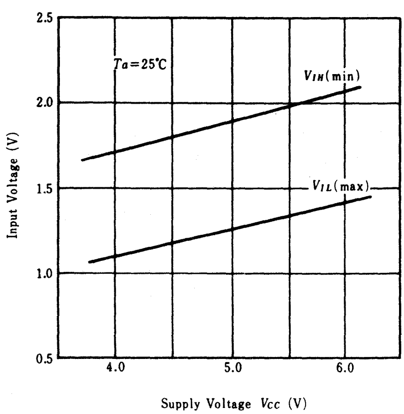
AVERAGE SUPPLY CURRENT vs. SUPPLY VOLTAGE



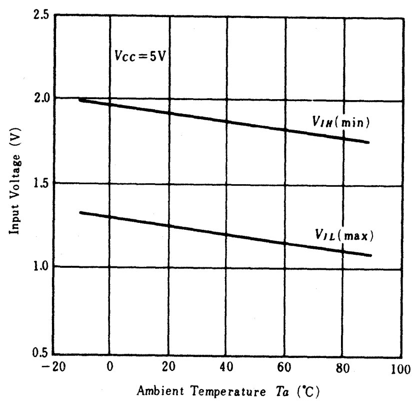
AVERAGE SUPPLY CURRENT vs. AMBIENT TEMPERATURE



INPUT VOLTAGE vs. SUPPLY VOLTAGE



INPUT VOLTAGE vs. AMBIENT TEMPERATURE

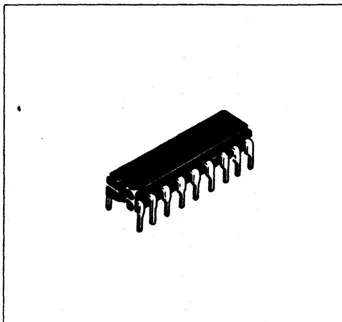


HM4334P-3L, HM4334P-4L

1024-word × 4-bit Static CMOS RAM

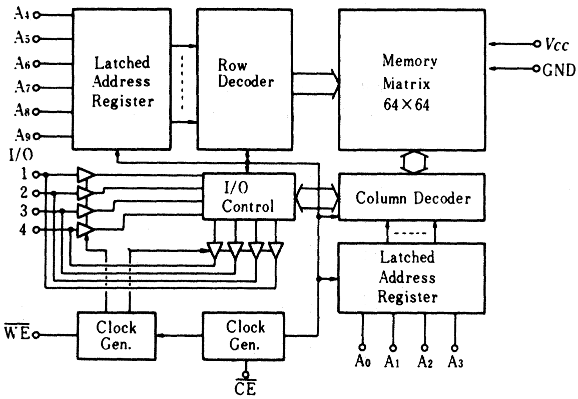
■FEATURES

- Single 5V Supply
- Low Power Standby and Low Power Operation; — Standby: 10μW (typ.), Operation: 20mW (typ.)
- Fast Access Time; HM4334P-3L: 300 ns (max.) (5V±5%); HM4334P-4L: 450 ns (max.) (5V±10%)
- Directly TTL Compatible: All inputs and outputs
- Common Data Input and Output using Three-state Outputs
- On Chip Address Register

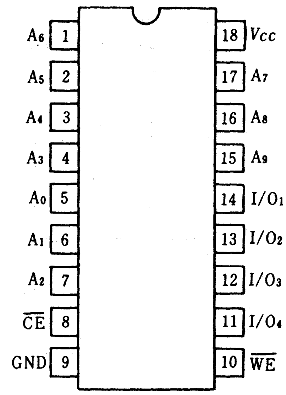


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage On Any Pin*	V_T	−0.3 to V_{CC}+0.5	V
Power Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃

* with respect to GND

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70℃)

Item	Symbol	HM4334P-3L			HM4334P-4L			Unit
		min	typ	max	min	typ	max	
Supply Voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
	GND	0	0	0	0	0	0	V
Input Voltage	V_{IH}	2.4	—	V_{CC}+0.5	2.4	—	V_{CC}+0.5	V
	V_{IL}	−0.3	—	0.8	−0.3	—	0.8	V

■DC AND OPERATING CHARACTERISTICS

(Ta=0 to +70°C, GND=0V, HM4334P-3L : V_{CC}=5V±5%, HM4334P-4L : V_{CC}=5V±10%)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	−1.0	—	+1.0	μA
Output Leakage Current	I_{LO}	$\overline{CE}=V_{IH}$, V_{out}=0 to V_{CC}	−1.0	—	+1.0	μA
Operating Power Supply Current	I_{CC1}	$\overline{CE}$=0V, $V_{IN}=V_{CC}$, $I_{I/O}$=0	—	—	1.0	mA
	I_{CC2}	$\overline{CE}$=0.8V, V_{IN}=2.4V, $I_{I/O}$=0	—	2.5	5.0	mA
Average Operating Current	I_{CC3}	V_{IN}=0 or V_{CC}, f=1MHz, duty 50%, $I_{I/O}$=0	—	4	7	mA
Standby Power Supply Current	I_{CCL}	$\overline{CE} \geqq V_{CC}-0.2V$	—	2	20	μA
Output Voltage	V_{OL}	I_{OL}=2.0mA	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

■CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Condition	min	typ	max	Unit
I/O Terminal Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	10	pF
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF

■AC CHARACTERISTICS

(Ta=0 to +70°C, GND=0V, HM4334P-3L : V_{CC}=5V±5%, HM4334P-4L : V_{CC}=5V±10%)

Item	Symbol		HM4334P-3L			HM4334P-4L			Unit
			min	typ	max	min	typ	max	
Read or Write Cycle Time*	TELEL	t_C	460	—	—	640	—	—	ns
Chip Enable Access Time	TELQV	t_{AC}	—	—	300	—	—	450	ns
Chip Enable to Output Active	TELQX	t_{CX}	50	—	—	50	—	—	ns
Output 3-state from Deselection	TEHQZ	t_{OFF1}	—	—	100	—	—	100	ns
Write Enable Output Disable Time	TWLQZ	t_{OFF2}	—	—	100	—	—	100	ns
Chip Enable Pulse Width**	TELEH	t_{CE}	300	—	—	450	—	—	ns
Chip Enable Precharge Time	TEHEL	t_P	120	—	—	150	—	—	ns
Address Hold Time	TELAX	t_{AH}	100	—	—	100	—	—	ns
Address Setup Time	TAVEL	t_{AS}	20	—	—	20	—	—	ns
Read Setup Time	TWHEL	t_{RS}	0	—	—	0	—	—	ns
Read Hold Time	TEHWL	t_{RH}	0	—	—	0	—	—	ns
Write Enable Setup Time	TWLEL	t_{WS}	−20	—	—	−20	—	—	ns
$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	TWLEH	t_{WPL}	300	—	—	450	—	—	ns
Chip Enable to Write Enable Delay Time	TELWL	t_{CWD}	300	—	—	450	—	—	ns
Write Enable Hold Time	TEHWH	t_{EWH}	0	—	—	0	—	—	ns
Write Hold Time	TELWH	t_{WH}	300	—	—	450	—	—	ns
Data Input Setup Time	TDVWH TDVEH	t_{DS}	200	—	—	350	—	—	ns
Data Hold Time	TWHDX TEHDX	t_{DH}	0	—	—	0	—	—	ns
Write Data Delay Time	TWLDV	t_{WDS}	100	—	—	100	—	—	ns
Chip Enable Rise/Fall Time	TT	t_T	—	—	300	—	—	300	ns

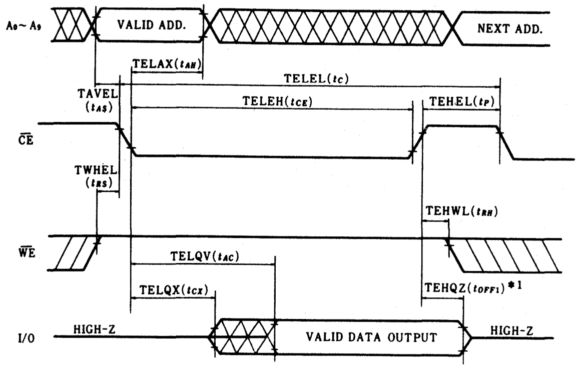
* TELEL (t_C)=TELEH (t_{CE})+TEHEL (t_P)+t_r(20ns)+t_f(20ns)

** For Read Modify Write Cycle, TELEH (t_{CE})=TELWL (t_{CWD})+TWLEH (t_{WPL})+t_f(20ns)

■AC TEST CONDITIONS

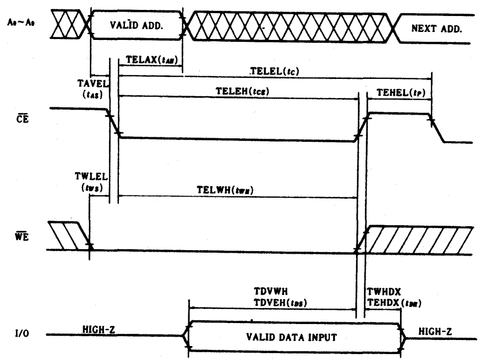
Input Level 2.4V, 0.8V
Input Rise and Fall Time 20ns
Timing Measurement Level 2.4V, 0.8V
Reference Level .... V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load .... 1 TTL and C_L = 100pF

● READ CYCLE



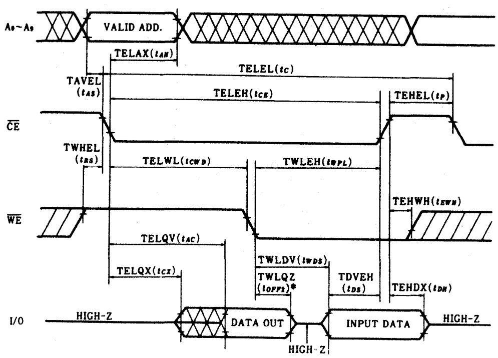
NOTE) *: T_{EHQZ} (t_{OFF_1}) defines the time at which the outputs achieve the open circuit condition and is not referenced to outputs voltage level.

● WRITE CYCLE



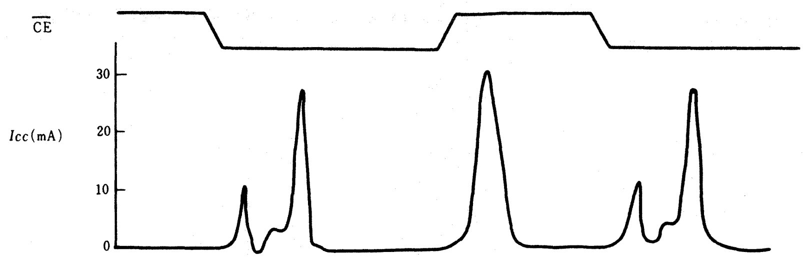
NOTE) t_{DS} and t_{DH} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

● READ MODIFY WRITE CYCLE



NOTE) *: T_{WLQZ} (t_{OFF_2}) defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

● CURRENT WAVEFORM



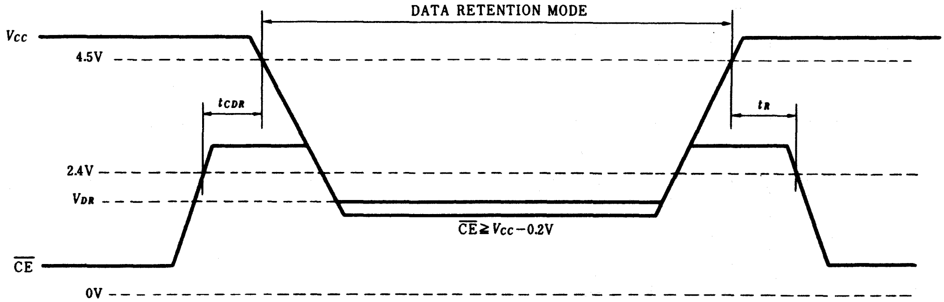
[NOTE] V_{CC} = 5.0V, T_a = 25°C

■ LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

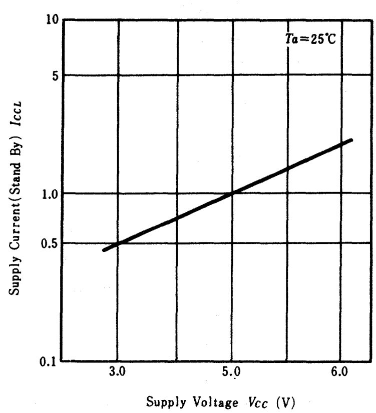
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Power Supply Current	I_{CCDR}	V_{DR}=3.0V	—	0.5	10	μA
Chip Deselection to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*	—	—	ns

* t_{RC}=Read Cycle Time

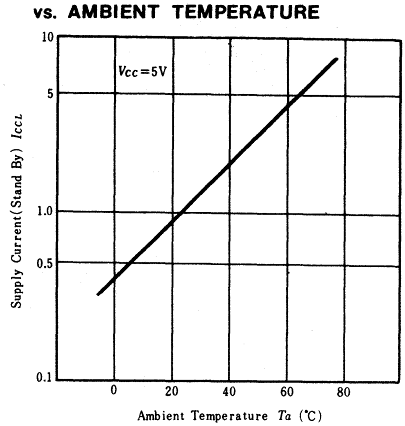
● LOW Vcc DATA RETENTION TIMING



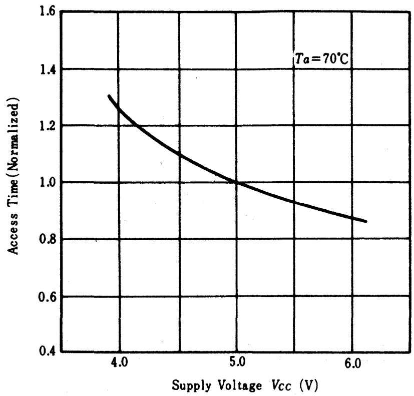
SUPPLY CURRENT (Standby) vs. SUPPLY VOLTAGE



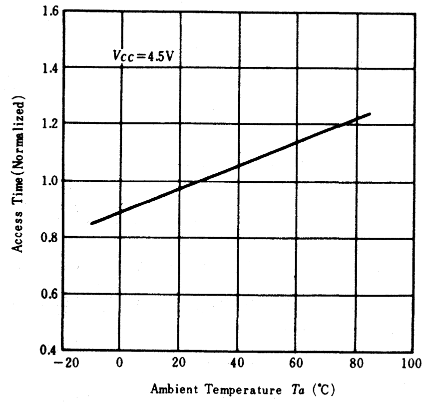
SUPPLY CURRENT (Standby) vs. AMBIENT TEMPERATURE



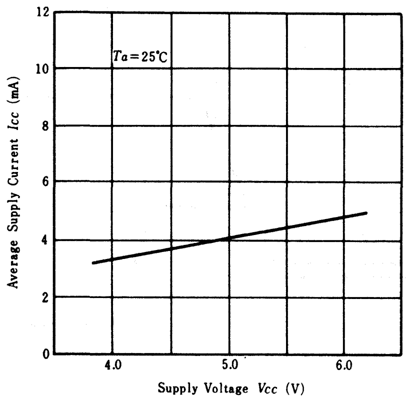
ACCESS TIME vs. SUPPLY VOLTAGE



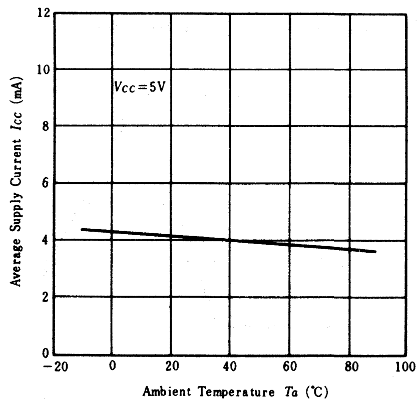
ACCESS TIME vs. AMBIENT TEMPERATURE



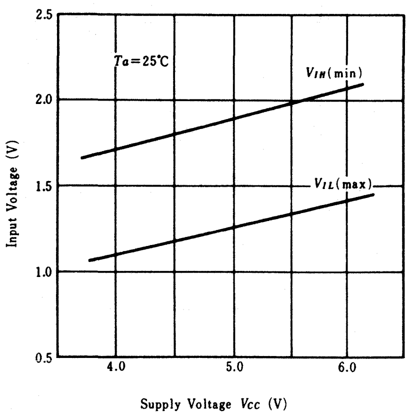
AVERAGE SUPPLY CURRENT vs. SUPPLY VOLTAGE



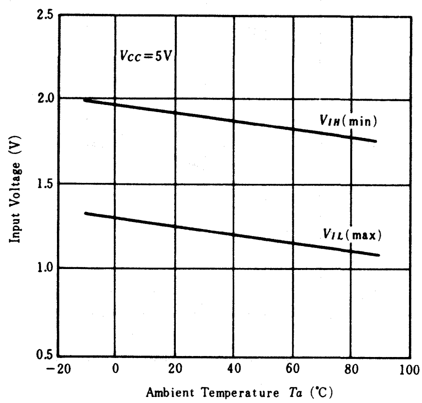
AVERAGE SUPPLY CURRENT vs. AMBIENT TEMPERATURE



INPUT VOLTAGE vs. SUPPLY VOLTAGE



INPUT VOLTAGE vs. AMBIENT TEMPERATURE



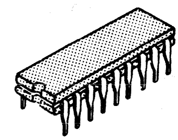
HM6148, HM6148-6
HM6148P, HM6148P-6

1024-word × 4-bit High Speed CMOS RAM

■FEATURES

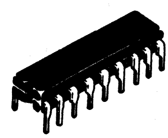
- Single 5V Supply
- Fast Access Time .... HM6148/P 70 ns (max.)
  HM6148/P-6 85 ns (max.)
- Low Power Standby and Low Power Operation; Standby: 100μW (typ) Operation: 200mW (typ)
- Completely Static RAM; No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Three State Output
- Common Data Input and Output
- Pin-Out Compatible with Intel 2148

HM6148, HM6148-6



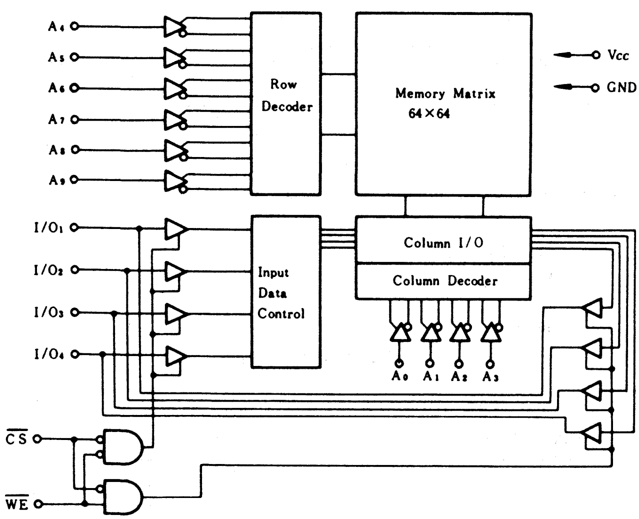
(DG-18)

HM6148P, HM6148P-6

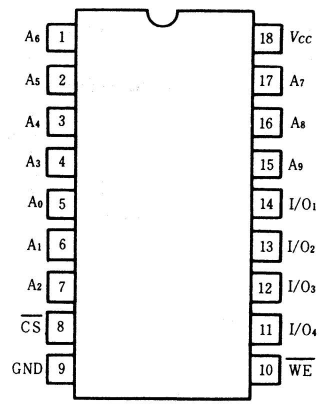


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage*	V_T	−0.5△to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature (Plastic)	T_{stg}	−55 to +125	℃
Storage Temperature (Cerdip)	T_{stg}	−65 to +150	℃
Storage Temperature**	$T_{stg(bias)}$	−10 to +85	℃

* with respect to GND. △ −1.0V (Pulse Width ≦ 50ns)
** Under Bias

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.4	3.5	6.0	V
	V_{IL}	−0.3*	—	0.8	V

* V_{IL} min=−1.0V (Pulse width≦50ns)

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	80	mA
	I_{CC1}	$\overline{CS}=V_{IL}$, Minimum Cycle, Duty=100%, $I_{I/O}$=0mA	—	40	80	mA
Average Operating Current	I_{CC2}**	Cycle=150ns, Duty=50%, $I_{I/O}$=0mA	—	35	—	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	12	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2V$, $V_{in}\leqq 0.2V$ or $V_{in}\geqq V_{CC}-0.2V$	—	20	800	μA
Output Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
	V_{OH}	I_{OH}=−3.2mA	2.4	—	—	V

Notes) * Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.
** Reference only.

■CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Condition	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	12	pF

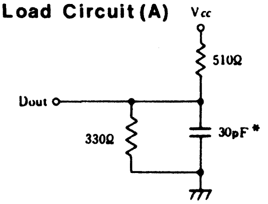
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C, unless otherwise noted)

●AC TEST CONDITIONS

Input Pulse Levels .... GND to 3.0V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels 1.5V
Output Load .... See Figure 1

Load Circuit (A)



* includes probe and jig capacitance

Load Circuit (B)

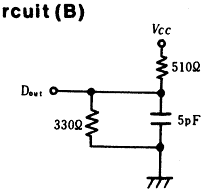


Fig. 1

■READ CYCLE

Parameter	Symbol	HM6148/P		HM6148/P-6		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	70	—	85	—	ns
Address Access Time	t_{AA}	—	70	—	85	ns
Chip Select Access Time	t_{ACS}	—	70	—	85	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z*	t_{LZ}	10	—	10	—	ns
Chip Deselection to Output in High Z*	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	40	—	40	ns

* Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

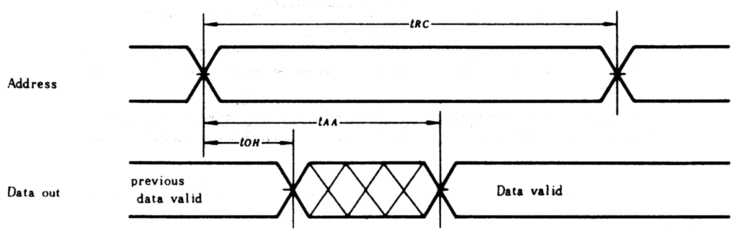
■WRITE CYCLE

Parameter	Symbol	HM6148/P		HM6148/P-6		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	70	—	85	—	ns
Chip Selection to End of Write	t_{CW}	50	—	60	—	ns
Address Valid to End of Write	t_{AW}	65	—	80	—	ns
Address Setup Time	t_{AS}	15	—	15	—	ns
Write Pulse Width*	t_{WP1}	50	—	60	—	ns
	t_{WP2}	65	—	80	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	ns
Data Valid to End of Write	t_{DW}	30	—	35	—	ns
Data Hold Time	t_{DH}	5	—	5	—	ns
Write Enabled to Output in High Z**	t_{WZ}	0	35	0	45	ns
Output Active from End of Write**	t_{OW}	0	—	0	—	ns

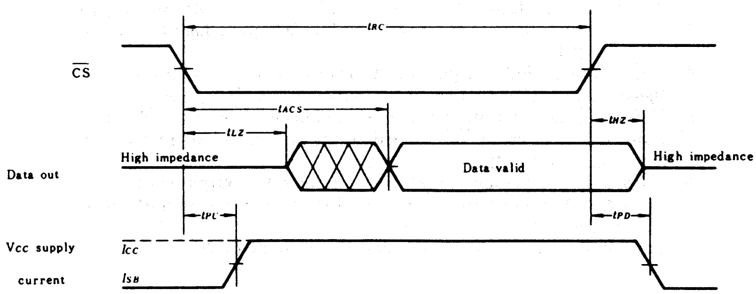
Notes) * When the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, I/O pins remain in a high impedance state. In this case t_{WP1}, in the other case t_{WP2} $(=t_{WZ}+t_{DW})$.

** Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

●TIMING WAVEFORM OF READ CYCLE NO.1 (1) (2)

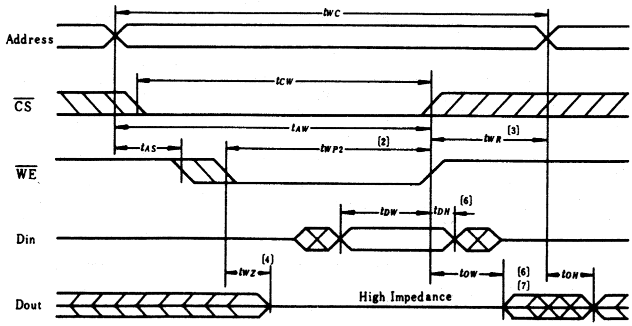


●TIMING WAVEFORM OF READ CYCLE NO.2 (1) (3)

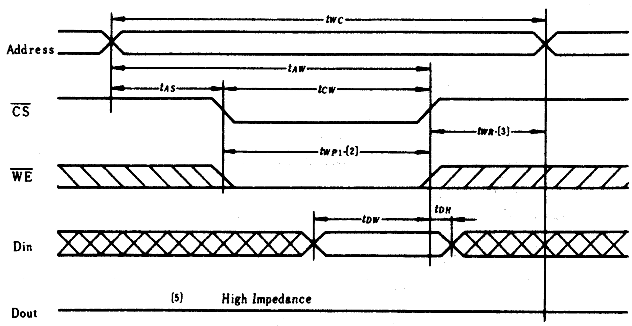


NOTES) 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$
3. Address Valid prior to or coincident with $\overline{CS}$ transition low.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED)[1]

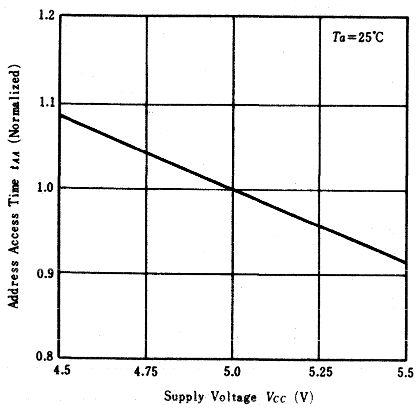


● TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED)[1]

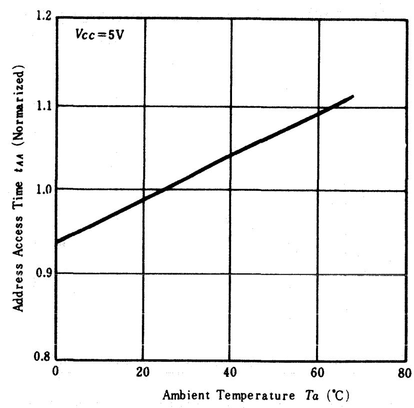


Notes)
1. $\overline{CS}$ and $\overline{WE}$ are paced in the WRITE state during low level period (t_W).
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
6. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
7. Dout is the same phase of write data of this write cycle.

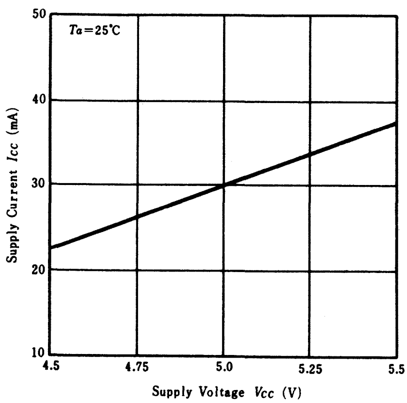
ACCESS TIME vs. V_{CC}



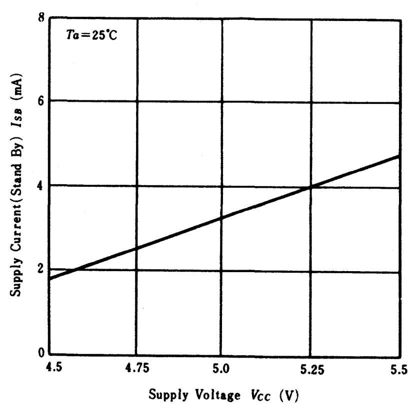
ACCESS TIME vs. Ta



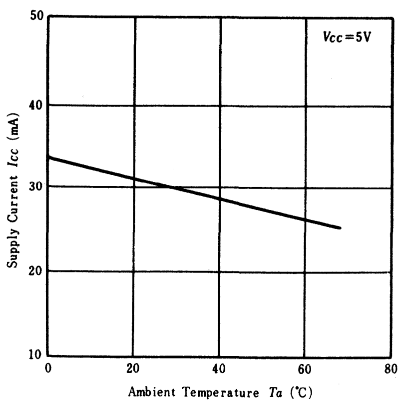
SUPPLY CURRENT vs. V_{CC}



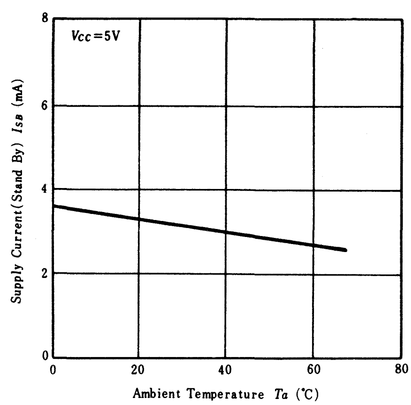
SUPPLY CURRENT vs. V_{CC}



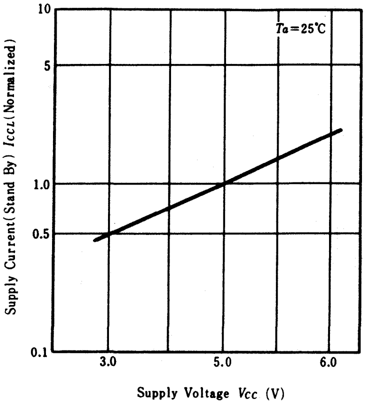
SUPPLY CURRENT vs. Ta



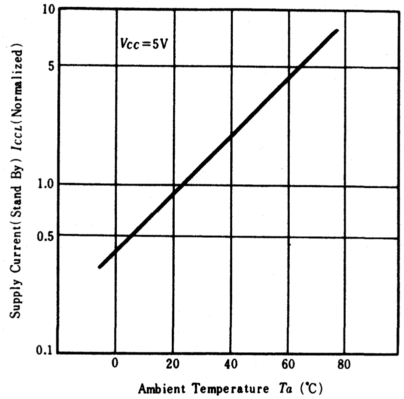
SUPPLY CURRENT vs. Ta



SUPPLY CURRENT vs. V_{cc} (STANDBY)

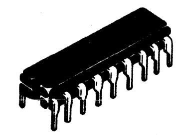


SUPPLY CURRENT vs. Ta (STANDBY)



HM6148LP, HM6148LP-6

1024-word × 4-bit High Speed Static CMOS RAM

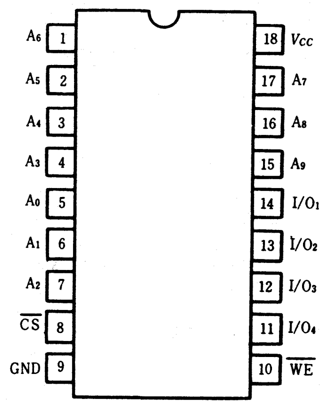


(DP-18)

■FEATURES

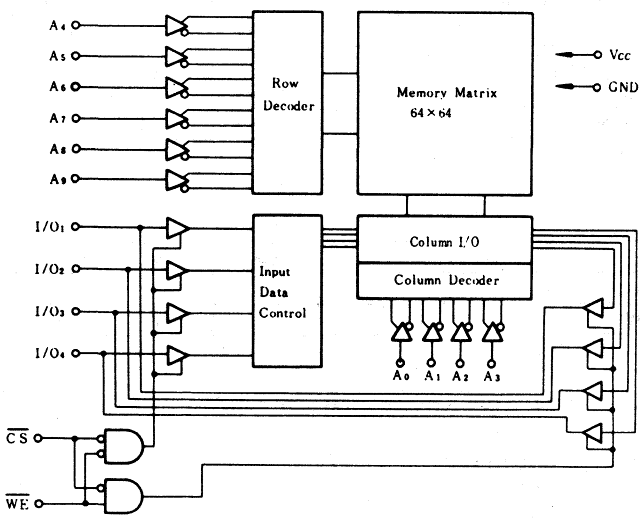
- Single 5V Supply
- Fast Access Time .... HM6148LP 70 ns (max.)
  HM6148LP-6 85 ns (max.)
- Low Power Standby and Low Power Operation;
  Standby: 5μW (typ) Operation: 200mW (typ)
- Completely Static RAM; No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Three State Output
- Common Data Input and Output
- Capability of Battery Back Up Operation
- Pin-Out Compatible with Intel 2148

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Terminal Voltage*	V_T	−0.5△to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃
Storage Temperature**	$T_{stg(bias)}$	−10 to +85	℃

* with respect to GND. △ −1.0V (Pulse Width ≦ 50ns)
** Under Bias

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item		Symbol	min	typ	max	Unit
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
		GND	0	0	0	V
Input Voltage		V_{IH}	2.4	3.5	6.0	V
		V_{IL}	−0.3*	—	0.8	V

* V_{IL} min=−1.0V (Pulse width≦50ns)

DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	80	mA
Average Operating Current	I_{CC1}	$\overline{CS}=V_{IL}$, Minimum Cycle, Duty=100%, $I_{I/O}$=0mA	—	40	80	mA
	I_{CC2}**	Cycle=150ns, Duty=50%, $I_{I/O}$=0mA	—	35	—	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	12	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{in} \leqq 0.2V$ or $V_{in} \geqq V_{CC}-0.2V$	—	1	100	μA
Output Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
	V_{OH}	I_{OH}=−3.2mA	2.4	—	—	V

Notes) * Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.
** Reference only.

CAPACITANCE (Ta=25°C, f=1MHz)

Item	Symbol	Test Condition	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	12	pF

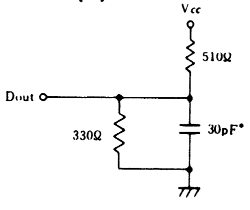
Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C, unless otherwise noted)

● AC TEST CONDITIONS

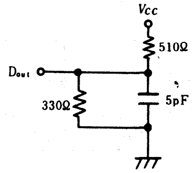
Input Pulse Levels .... GND to 3.0V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels 1.5V
Output Load .... See Figure

Load Circuit (A)



* includes probe and jig capacitance.

Load Circuit (B)



● READ CYCLE

Parameter	Symbol	HM6148LP		HM6148LP-6		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	70	—	85	—	ns
Address Access Time	t_{AA}	—	70	—	85	ns
Chip Select Access Time	t_{ACS}	—	70	—	85	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z*	t_{LZ}	10	—	10	—	ns
Chip Deselection to Output in High Z*	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	40	—	40	ns

* Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

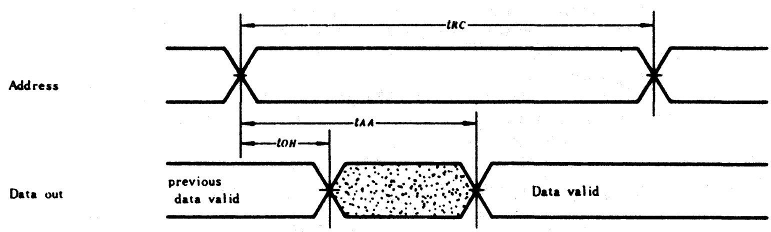
● WRITE CYCLE

Parameter	Symbol	HM6148LP		HM6148LP-6		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	70	—	85	—	ns
Chip Selection to End of Write	t_{CW}	50	—	60	—	ns
Address Valid to End of Write	t_{AW}	65	—	80	—	ns
Address Setup Time	t_{AS}	15	—	15	—	ns
Write Pulse Width*	t_{WP1}	50	—	60	—	ns
	t_{WP2}	65	—	80	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	ns
Data Valid to End of Write	t_{DW}	30	—	35	—	ns
Data Hold Time	t_{DH}	5	—	5	—	ns
Write Enabled to Output in High Z**	t_{WZ}	0	35	0	45	ns
Output Active from End of Write**	t_{OW}	0	—	0	—	ns

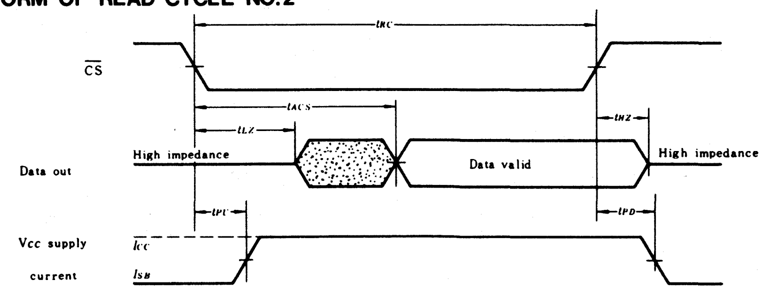
Notes) * When the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, I/O pins remain in a high impedance state. In this case t_{WP1}, in the other case t_{WP2} $(=t_{WZ}+t_{DW})$.

** Transition is measured ±500mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO.1 (1) (2)

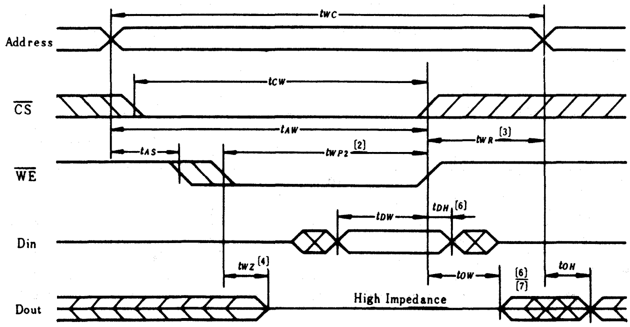


● TIMING WAVEFORM OF READ CYCLE NO.2 (1) (3)

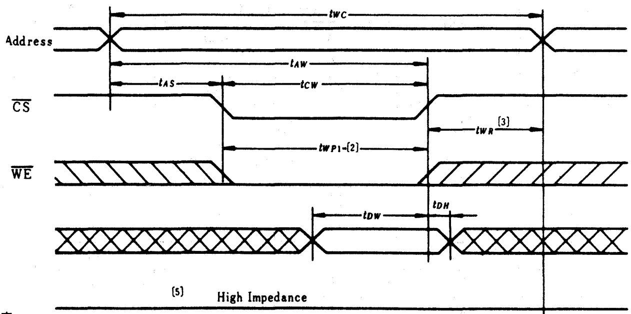


Notes) 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}=V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition low.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED)(1)



● TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED)(1)



Notes)

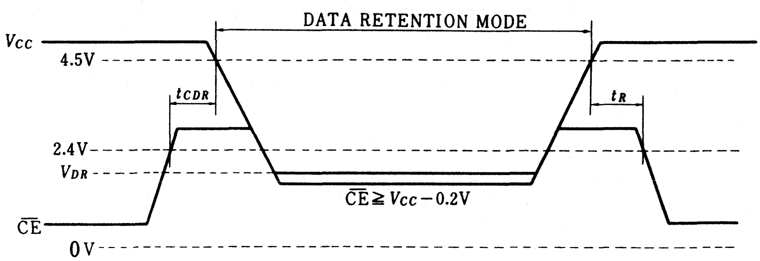
1. $\overline{CS}$ and $\overline{WE}$ are paced in the WRITE state during low level period (t_W).
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
6. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
7. Dout is the same phase of write data of this write cycle.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

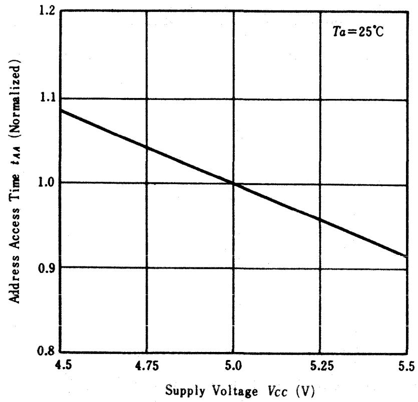
Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{CC}=2.0V$, $\overline{CS} \geq 1.8V$, $V_{in}=1.8V$ or $V_{in} \leq 0.2V$	—	—	40	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*	—	—	ns

* t_{RC} = Read Cycle Time

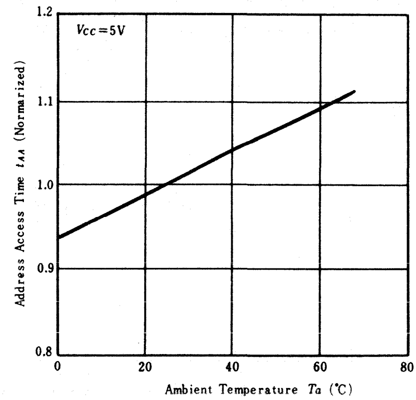
● LOW V_{CC} DATA RETENTION WAVEFORM



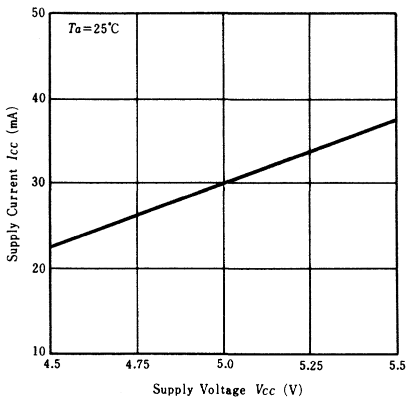
ACCESS TIME vs. Vcc



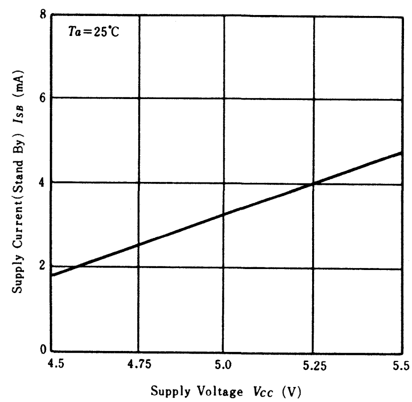
ACCESS TIME vs. Ta



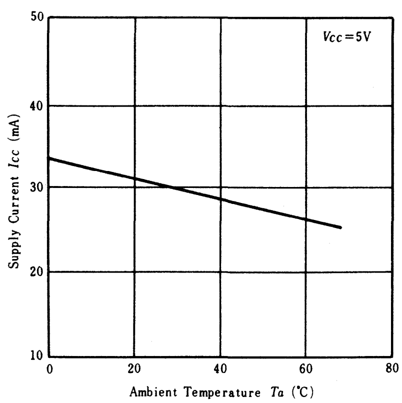
SUPPLY CURRENT vs. Vcc



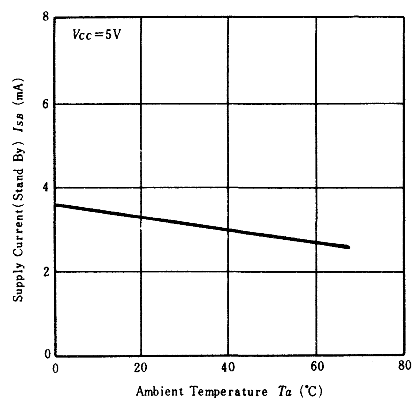
SUPPLY CURRENT vs. Vcc



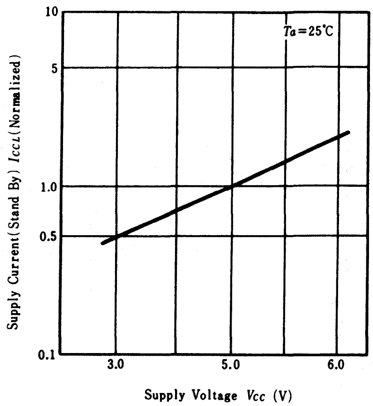
SUPPLY CURRENT vs. Ta



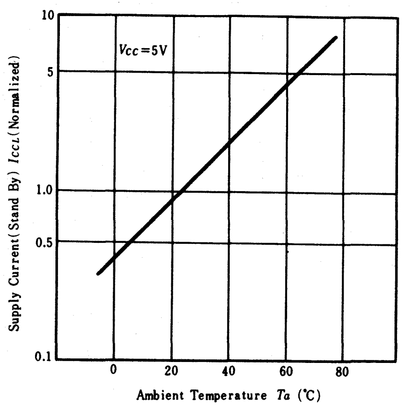
SUPPLY CURRENT vs. Ta



SUPPLY CURRENT vs. V_{CC} (STANDBY)



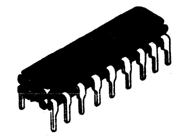
SUPPLY CURRENT vs. Ta (STANDBY)



HM4315P

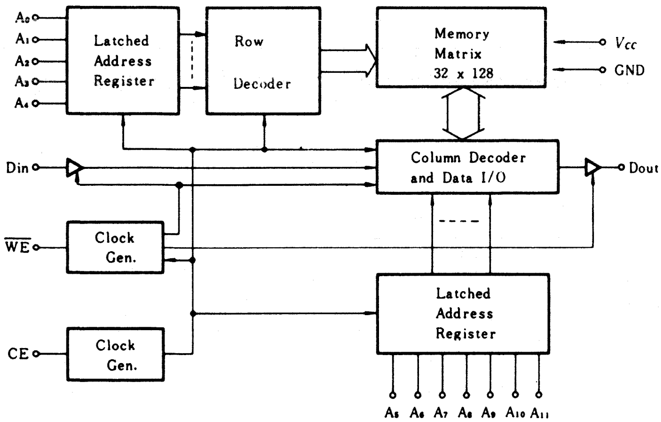
4096-word × 1-bit Static Random Access Memory

- Low Power Standby .... 10μW typ.
- Low Power Operation .... 20mW typ.
- Data Retention 2.0V
- Access Time .... 450 ns max.
- TTL/CMOS Compatible Input/Output
- On Chip Address Register
- Si Gate CMOS Technology

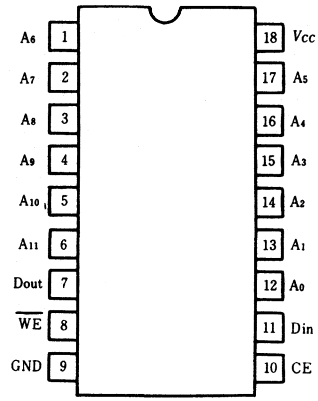


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Terminal Voltage*	V_T	−0.3 to V_{CC}+0.3	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃

* with respect to GND

■RECOMMENDED DC OPERATING CONDITION (Ta=0 to +70℃)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.4	—	V_{CC}+0.3	V
	V_{IL}	−0.3	—	0.8	V

■DC AND OPERATING CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±10%)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=0~V_{CC}	−1.0	—	1.0	μA
Output Leakage Current	I_{LO}	CE=V_{IL}, V_{out}=0~V_{CC}	−1.0	—	1.0	μA
Operating Power Supply Current	I_{CC1}	CE=V_{CC}, V_{IN}=V_{CC} or 0V, Output Open	—	—	1.0	mA
	I_{CC2}	CE=2.4V, V_{IN}=2.4V, Output Open	—	2.5	5.0	mA
Average Power Supply Current	I_{CC3}	V_{IH}≧V_{CC}−0.2V, f=1MHz, duty 50%	—	4	10	mA
	I_{CC4}	V_{IH}=2.4V, f=1MHz, duty 50%	—	6	15	mA
Standby Power Supply Current	I_{CCL}	CE≦0.2V	—	2	100	μA
Output Voltage	V_{OL}	I_{OL}=2.0mA	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

■CAPACITANCE (Ta=25℃, f=1MHz)

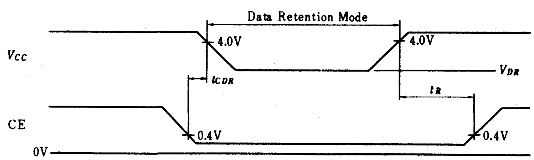
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	3	5	pF
Output Capacitance	C_{out}	V_{out}=0V	—	7	10	pF

■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70℃)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	CE≦0.2V	2.0	—	—	V
Data Retention Power Supply Current	I_{CCDR}	CE≦0.2V, V_{DR}=2.0V	—	0.5	50	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_C*	—	—	ns

* t_C=Cycle time

■LOW Vcc DATA RETENTION TIMING



■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃)

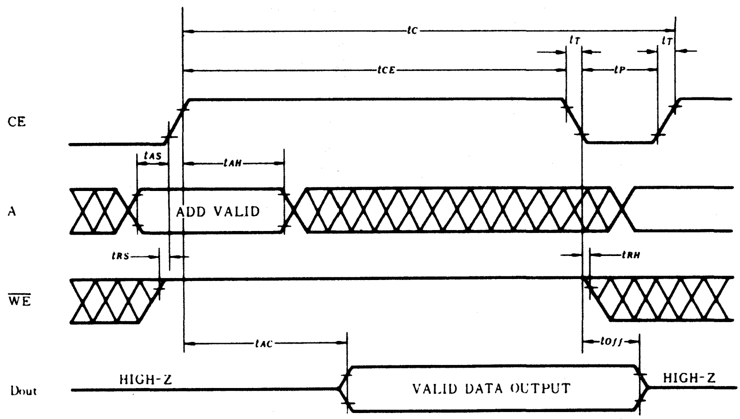
● AC TEST CONDITIONS

Input High Level 2.4V
Input Low Level 0.8V
Input Rise and Fall Times 20ns
Timing Measurement Levels 2.4V, 0.8V
Reference Level .... V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load .... 1 TTL + C_L = 100pF

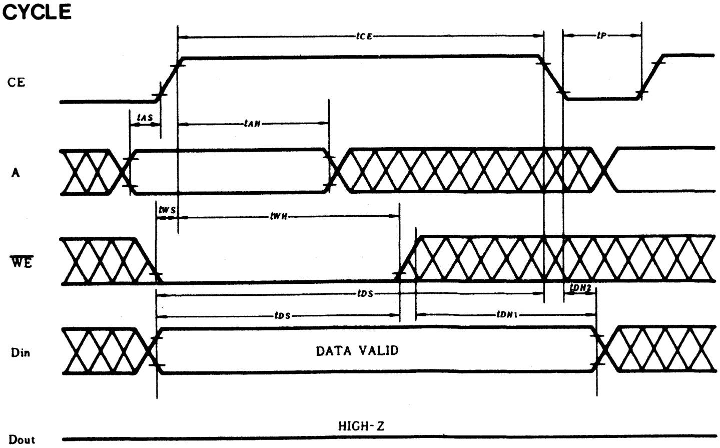
Item	Symbol	min	max	Unit
Read or Write Cycle Time	TEHEH (t_C)	640	—	ns
Random Access Time	TEHQV (t_{AC})	—	450	ns
Chip Enable Pulse Width	TEHEL (t_{CE})	450	—	ns
Chip Enable Precharge Time	TELEH (t_P)	150	—	ns
Address Hold Time	TEHAX (t_{AH})	200	—	ns
Address Setup Time	TAVEH (t_{AS})	20	—	ns
Output Buffer Turn-off Delay	TELQZ (t_{off})	0	100	ns
Write Enable Setup Time	TEHWL (t_{WS})	−20	—	ns
Data Input Hold Time	TWHDX (t_{DH1})	60	—	ns
Data Input Hold Time referenced to CE	TELDX (t_{DH2})	40	—	ns
Write Enable Pulse Width	TWLWH(t_{WW})	120	—	ns
Chip Enable to Write Enable Delay*	TEHWL (t_{CWD})	350	—	ns
$\overline{WE}$ to CE Precharge Lead Time	TWLEL (t_{WPL})	150	—	ns
Data Input Setup Time	TDVWH, TDVEL (t_{DS})	100	—	ns
Write Enable Hold Time	TEHWH (t_{WH})	300	—	ns
Read Setup Time	TWHEH (t_{RS})	0	—	ns
Read Hold Time	TELWL (t_{RH})	0	—	ns
Chip Enable Rise/Fall Time	TT(t_T)	—	300	ns

* Read-Modify-Write Cycle.

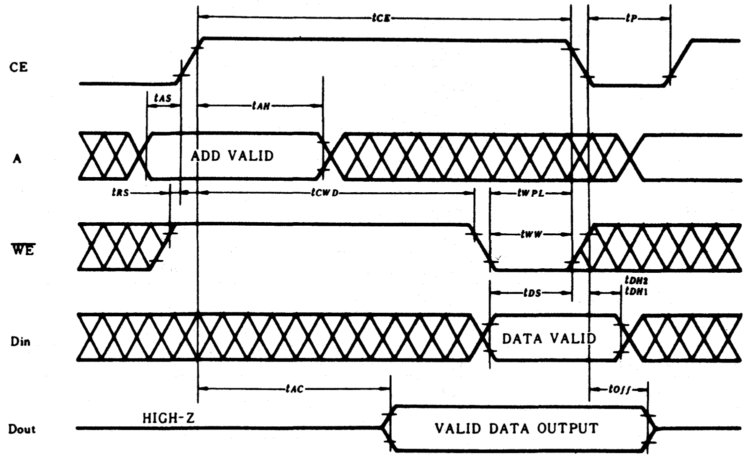
● READ CYCLE



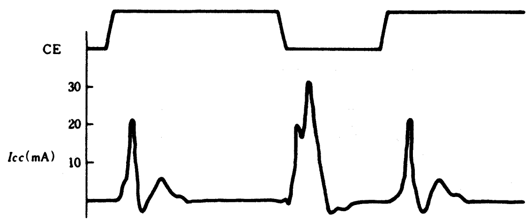
● EARLY WRITE CYCLE



● READ MODIFY WRITE CYCLE AND READ WRITE CYCLE

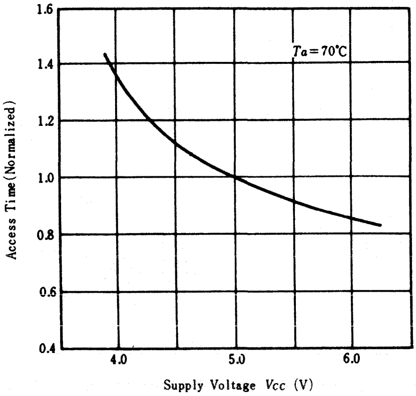


Notes) ＊1 Read-Modify-Write Cycle $t_{CWD} \geqq 350$ns, $t_{CE} = 550$ns.
＊2 Read-Write Cycle.

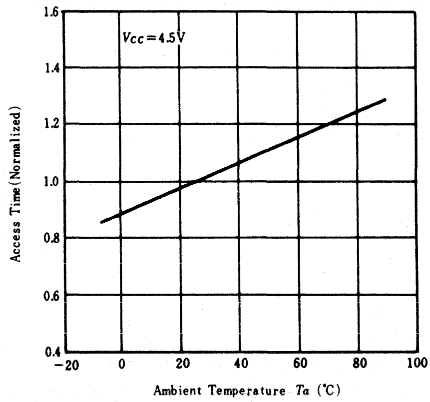


Note) $V_{CC} = 5.0$V, $Ta = 25$°C

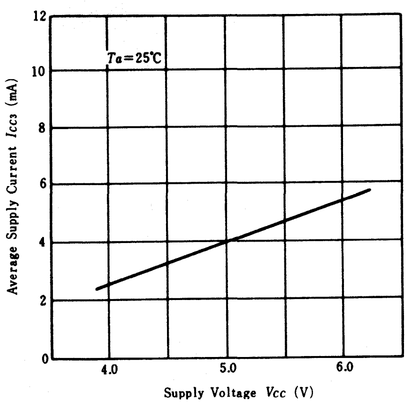
ACCESS TIME vs. SUPPLY VOLTAGE



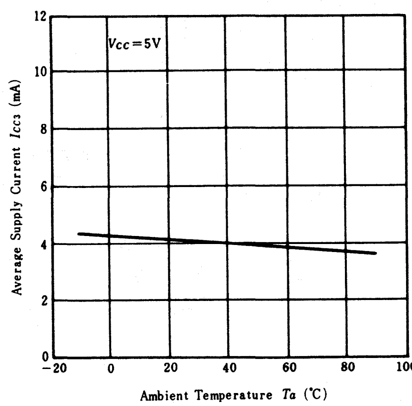
ACCESS TIME vs. AMBIENT TEMPERATURE



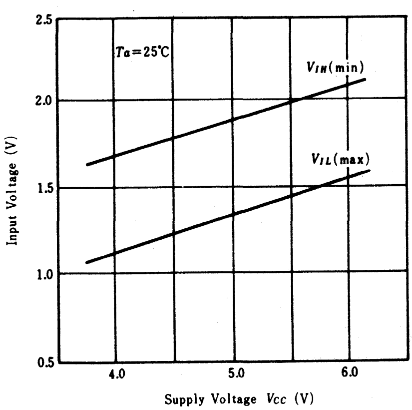
AVERAGE SUPPLY CURRENT vs. SUPPLY VOLTAGE



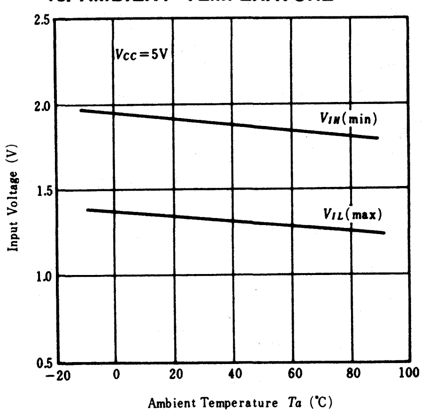
AVERAGE SUPPLY CURRENT vs. AMBIENT TEMPERATURE



INPUT VOLTAGE vs. SUPPLY VOLTAGE



INPUT VOLTAGE vs. AMBIENT TEMPERATURE



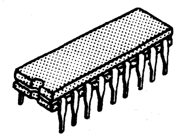
HM6147, HM6147-3
HM6147P, HM6147P-3

4096-word × 1-bit High Speed Static CMOS RAM

■FEATURES

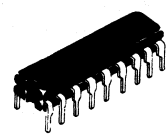
- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby: 100μW typ., Operation: 75mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

HM6147, HM6147-3



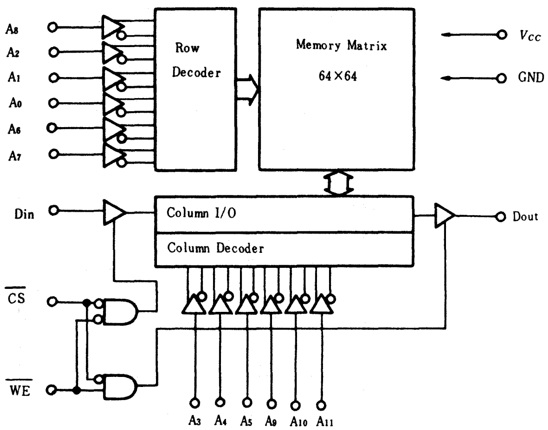
(DG-18)

HM6147P, HM6147P-3

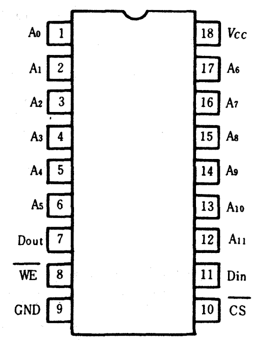


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	℃
Storage Temperature (Plastic)	T_{stg}	−55 to +125	℃

* V_{IN} min = −1.0V (Pulse Width ≦ 20ns)

■RECOMMENDED DC OPERATING CONDITIONS (0℃ ≦ Ta ≦ 70℃)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} min = −1.0V (Pulse width ≦ 20ns)

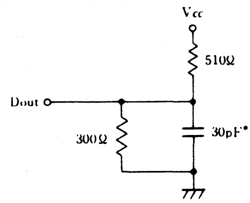
■DC AND OPERATING CHARACTERISTICS (0°C≦Ta≦70°C, V_{CC}=5V±10%, GND=0V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit	Notes
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, GND to V_{CC}	—	—	2.0	μA	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, V_{out}=0~V_{CC}	—	—	2.0	μA	
Operating Power Supply Current(1) DC	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	15	35	mA	
Operating Power Supply Current(2) DC	I_{CC1}	$\overline{CS}=V_{IL}$, V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	—	12	—	mA	[2]
Average Operating Current(3)	I_{CC2}	Cycle 150ns, duty 50%	—	14	—	mA	[2]
Standby Power Supply Current(1) DC	I_{SB}	$\overline{CS}=V_{IH}$	—	5	12	mA	
Standby Power Supply Current(2) DC	I_{SB1}	$\overline{CS}$≧V_{CC}−0.2V, V_{IN}≦0.2V or V_{IN}≧V_{CC}−0.2V	—	20	800	μA	
Output Low Voltage	V_{OL}	I_{OL}=12mA	—	—	0.40	V	
Output High Voltage	V_{OH}	I_{OH}=−8.0mA	2.4	—	—	V	

Note) 1. Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.
2. Reference only

■AC TEST CONDITIONS

- Input pulse levels: GND to 3.5V
- Input rise and fall times: 10 ns
- Input and output timing reference levels: 1.5V
- Output load: See Figure 1



* Including scope & jig capacitance
Figure 1 Output Load

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Conditions	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	5	pF
Output Capacitance	C_{out}	V_{out}=0V	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0°C to 70°C, V_{CC}=5V±10%, unless otherwise noted.)

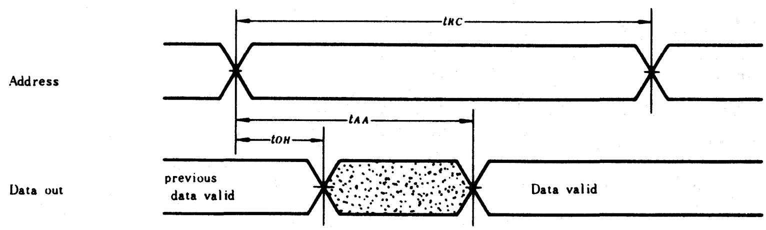
●READ CYCLE

Parameter	Symbol	HM6147/P-3		HM6147/P		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	55	—	70	—	ns
Address Access Time	t_{AA}	—	55	—	70	ns
Chip Select Access Time	t_{ACS}	—	55	—	70	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

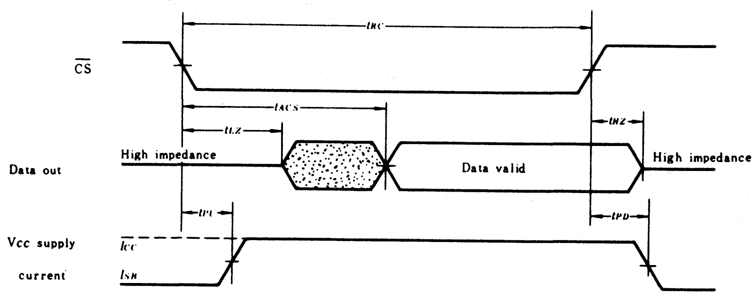
●WRITE CYCLE

Parameter	Symbol	HM6147/P-3		HM6147/P		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	55	—	70	—	ns
Chip Selection to End of Write	t_{CW}	45	—	55	—	ns
Address Valid to End of Write	t_{AW}	45	—	55	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	35	—	40	—	ns
Write Recovery Time	t_{WR}	10	—	15	—	ns
Data Valid to End of Write	t_{DW}	25	—	30	—	ns
Data Hold Time	t_{DH}	10	—	10	—	ns
Write Enabled to Output in High Z	t_{WZ}	0	30	0	35	ns
Output Active from End of Write	t_{OW}	0	—	0	—	ns

● TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2)

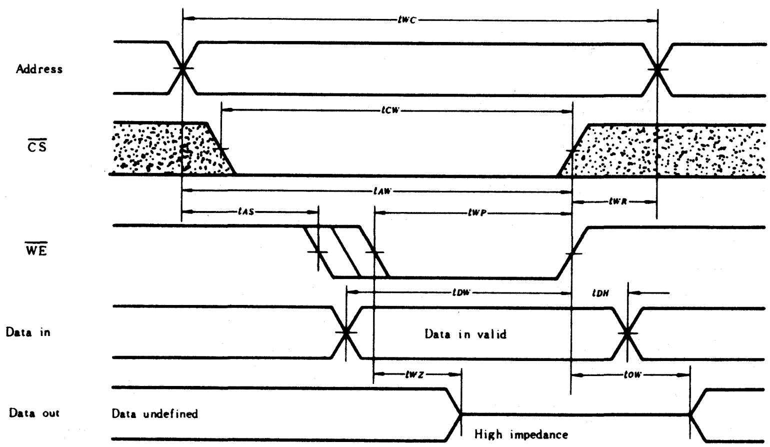


● TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)

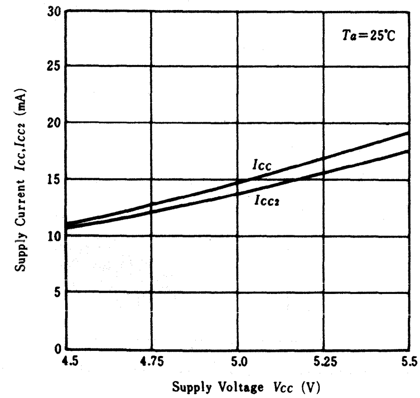


Notes: 1. $\overline{WE}$ is high for READ Cycle.
2. $\overline{CS}$ is low for READ Cycle.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

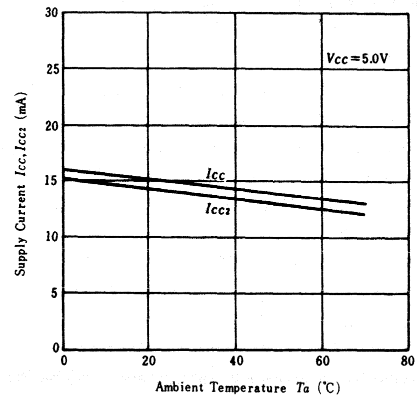
● TIMING WAVEFORM OF WRITE CYCLE



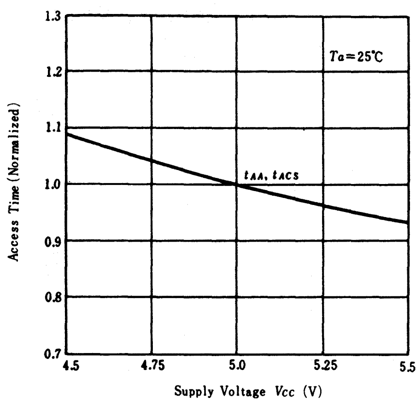
SUPPLY CURRENT vs. SUPPLY VOLTAGE



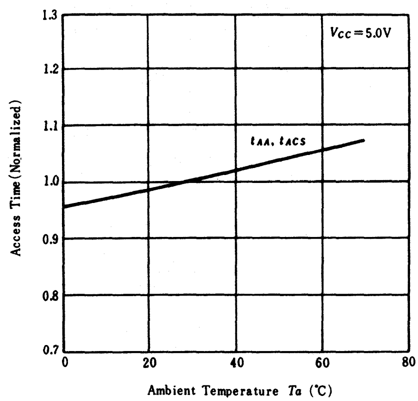
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



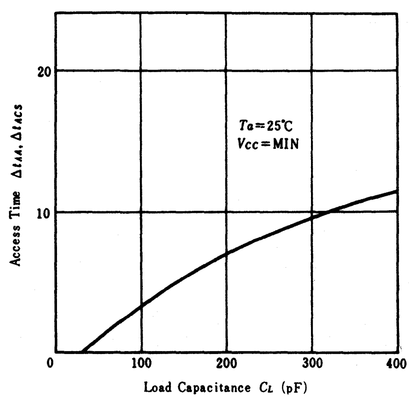
ACCESS TIME vs. SUPPLY VOLTAGE



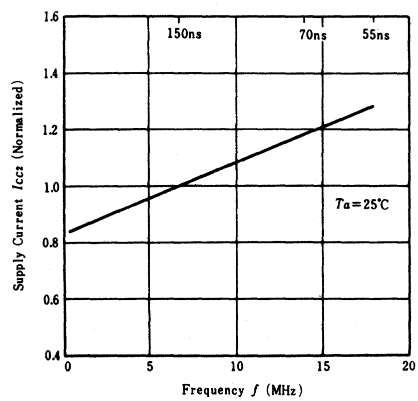
ACCESS TIME vs. AMBIENT TEMPERATURE



ACCESS TIME vs. LOAD CAPACITANCE



SUPPLY CURRENT vs. FREQUENCY

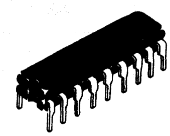


HM6147LP, HM6147LP-3

4096-word×1-bit High Speed Static CMOS RAM

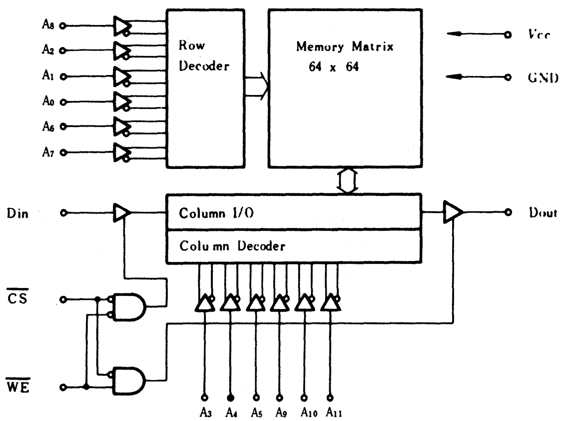
■FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation,
  Standby: 5μW typ. Operation: 75mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible – All Input and Output
- Separate Data Input and Output: Three State Output
- Capability of Battery Back up Operation
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

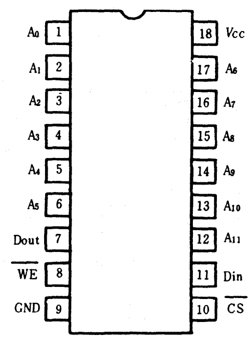


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND*	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃

* V_{IL} min = −1.0V (Pulse Width ≦ 20ns)

■RECOMMENDED DC OPERATING CONDITIONS (0℃ ≦ Ta ≦ 70℃)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} min = −1.0V (Pulse width ≦ 20ns)

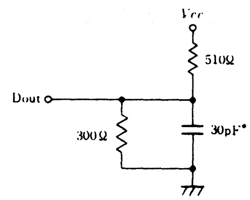
■DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5V\pm10\%$, GND=0V)

Parameter	Symbol	Test Condition	min	typ	max	Unit	Notes
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.5V$, GND to V_{CC}	—	—	2.0	μA	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, $V_{out}=0\sim V_{CC}$	—	—	2.0	μA	
Operating Power Supply Current(1) DC	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	15	35	mA	
Operating Power Supply Current(2) DC	I_{CC1}	$\overline{CS}=V_{IL}$, $V_{IN}\leq0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	—	12	—	mA	(2)
Average Operating Current(3)	I_{CC2}	Cycle 150ns, duty 50%	—	14	—	mA	(2)
Standby Power Supply Current(1) DC	I_{SB}	$\overline{CS}=V_{IH}$	—	5	12	mA	
Standby Power Supply Current(2) DC	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{IN}\leq0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	—	1	100	μA	
Output Low Voltage	V_{OL}	$I_{OL}=12mA$	—	—	0.40	V	
Output High Voltage	V_{OH}	$I_{OH}=-8.0mA$	2.4	—	—	V	

Note) 1. Typical limits are at $V_{CC}=5.0V$, $Ta=25°C$ and specified loading.
2. Reference only.

■AC TEST CONDITIONS

- Input pulse levels: GND to 3.5V
- Input rise and fall times: 10 ns
- Input and output timing reference levels: 1.5V
- Output load: See Figure 1



* Including scope & jig capacitance
Figure 1 Output Load

■CAPACITANCE ($Ta=25°C$, $f=1.0MHz$)

Item	Symbol	Condition	max	Unit
Input Capacitance	C_{in}	$V_{IN}=0V$	5	pF
Output Capacitance	C_{out}	$V_{out}=0V$	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS ($Ta=0°C$ to $70°C$, $V_{CC}=5V\pm10\%$, unless otherwise noted.)

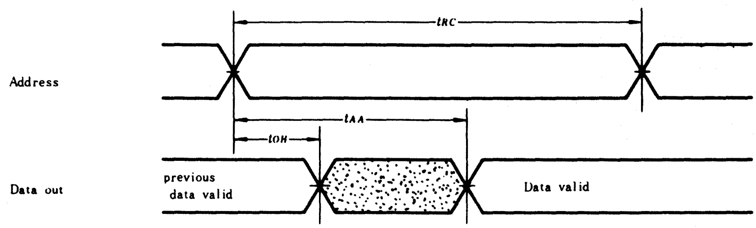
●READ CYCLE

Parameter	Symbol	HM6147LP-3		HM6147LP		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	55	—	70	—	ns
Address Access Time	t_{AA}	—	55	—	70	ns
Chip Select Access Time	t_{ACS}	—	55	—	70	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

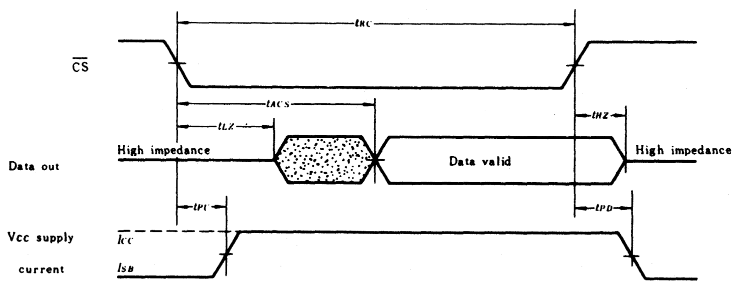
● WRITE CYCLE

Parameter	Symbol	HM6147LP-3		HM6147LP		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	55	—	70	—	ns
Chip Selection to End of Write	t_{CW}	45	—	55	—	ns
Address Valid to End of Write	t_{AW}	45	—	55	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	35	—	40	—	ns
Write Recovery Time	t_{WR}	10	—	15	—	ns
Data Valid to End of Write	t_{DW}	25	—	30	—	ns
Data Hold Time	t_{DH}	10	—	10	—	ns
Write Enabled to Output in High Z	t_{WZ}	0	30	0	35	ns
Output Active from End of Write	t_{OW}	0	—	0	—	ns

● TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2)

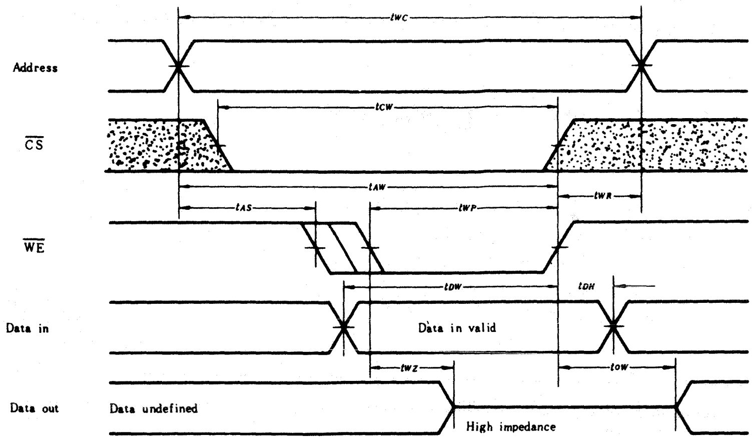


● TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)



NOTES: 1. $\overline{WE}$ is high for READ Cycle.
2. $\overline{CS}$ is low for READ Cycle.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

● TIMING WAVEFORM OF WRITE CYCLE

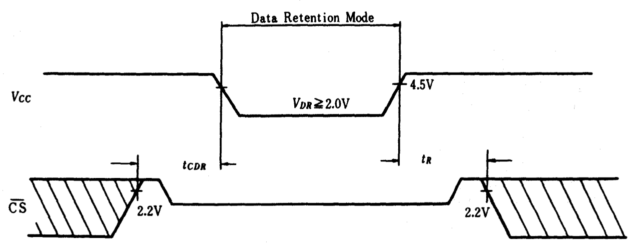


■ LOW V_{CC} RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{in} \geq V_{CC}-0.2V$ or $\leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{CC}=2.0V$, $\overline{CS} \geq 1.8V$, $V_{in} \geq 1.8V$ or $\leq 0.2V$	—	—	40	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*	—	—	ns

* t_{RC}=Read Cycle Time

● LOW V_{CC} RETENTION CHARACTERISTICS



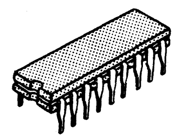
HM6147H-35, HM6147H-45-Preliminary
HM6147HP-35, HM6147HP-45

4096-word×1-bit High Speed Static CMOS RAM

■FEATURES

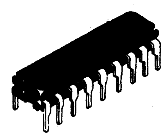
- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 35ns/45ns Max.
- Low Power Standby and Low Power Operation, Standby: 100μW typ., Operation: 150mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM

HM6147H-35, HM6147H-45



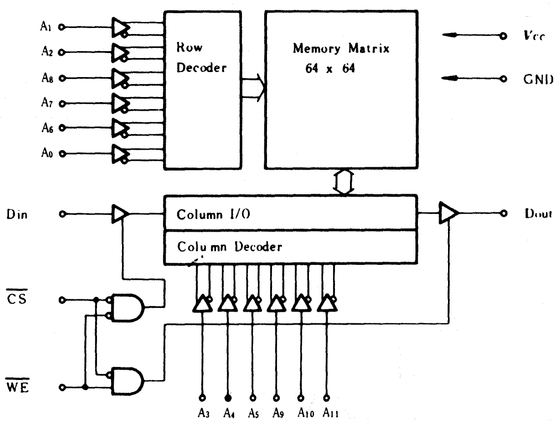
(DG-18)

HM6147HP-35, HM6147HP-45

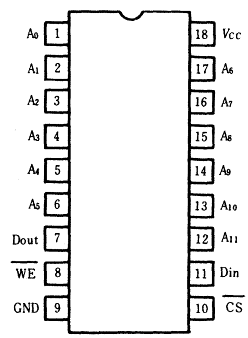


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	V_T	−3.5* to +7.0	V
DC Output Current	I_o	20	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature (under bias)	$T_{stg(bias)}$	−10 to +85	℃
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	℃
Storage Temperature (Plastic)	T_{stg}	−55 to +125	℃

* Pulse Width 20ns, DC : −0.5V

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■RECOMMENDED DC OPERATING CONDITIONS (0°C ≦ Ta ≦ 70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.0	3.0	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse Width 20ns, DC : −0.5V

■DC AND OPERATING CHARACTERISTICS (0°C ≦ Ta ≦ 70°C, V_{CC}=5V±10%, GND=0V)

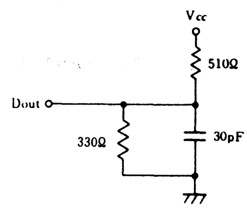
Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V, GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, V_{out}=0V~V_{CC}	—	—	2	μA
Operating Power Supply Current(1) DC	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	30	80	mA
Operating Power Supply Current(2) DC	I_{CC1}	$\overline{CS}=V_{IL}$, Minimum Cycle	—	40	80	mA
Standby Power Supply Current(1) DC	I_{SB}	$\overline{CS}=V_{IH}$, V_{CC}=Min to Max	—	8	20	mA
Standby Power Supply Current(2) DC	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	—	20	800	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.40	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet minute.
2. Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

■AC TEST CONDITIONS

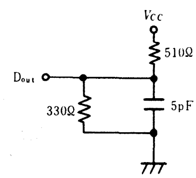
- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels: 1.5V (HM6147H/P-35)
  0.8 to 2.0V (HM6147H/P-45)

Output Load A



* Including scope & jig capacitance

Output Load B



■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Conditions	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	5	pF
Output Capacitance	C_{out}	V_{out}=0V	6	pF

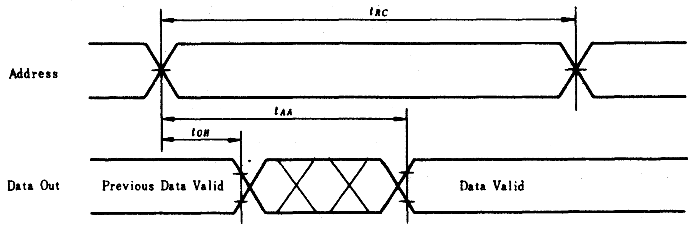
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0°C to 70°C, V_{CC}=5V±10%, unless otherwise noted.)

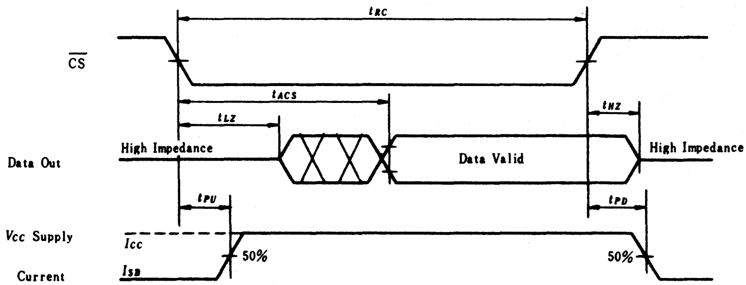
● READ CYCLE

Parameter	Symbol	HM6147H/P-35		HM6147H/P-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	ns	(1)
Address Access Time	t_{AA}	—	35	—	45	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	(2), (3), (7)
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	(2), (3), (7)
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	ns	

● TIMING WAVEFORM OF READ CYCLE NO.1 (4) (5)



● TIMING WAVEFORM OF READ CYCLE NO.2 (4) (6)

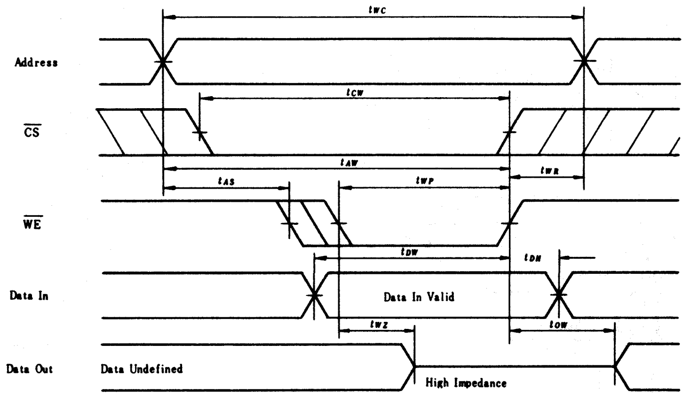


Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, $\overline{CS}=V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

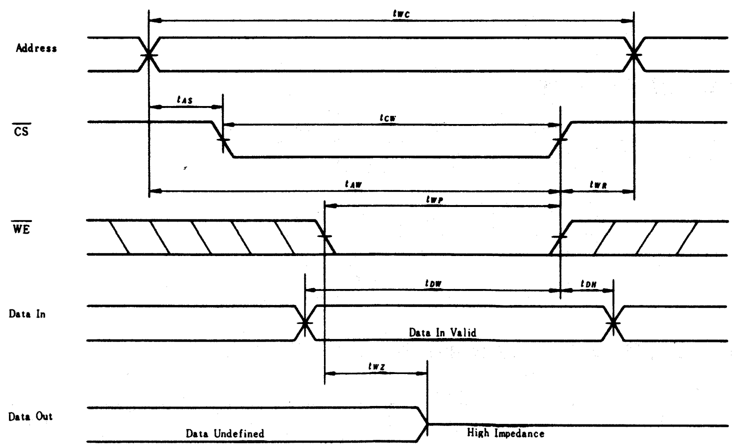
● WRITE CYCLE

Parameter	Symbol	HM6147H/P-35		HM6147H/P-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	ns	[2]
Chip Selection to End of Write	t_{CW}	35	—	45	—	ns	
Address Valid to End of Write	t_{AW}	35	—	45	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{DH}	10	—	10	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	ns	[3], [4]
Output Active from End of Write	t_{OW}	0	—	0	—	ns	[3], [4]

● TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ CONTROLLED)



● TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ CONTROLLED)



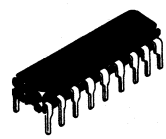
Note) $\overline{CS}$ or $\overline{WE}$ are High for Address Transition

Notes: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

HM6147HLP-35, HM6147HLP-45

—Preliminary—

4096-word × 1-bit High Speed Static CMOS RAM

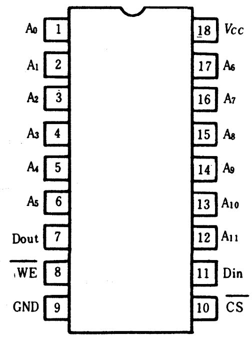


(DP-18)

■FEATURES

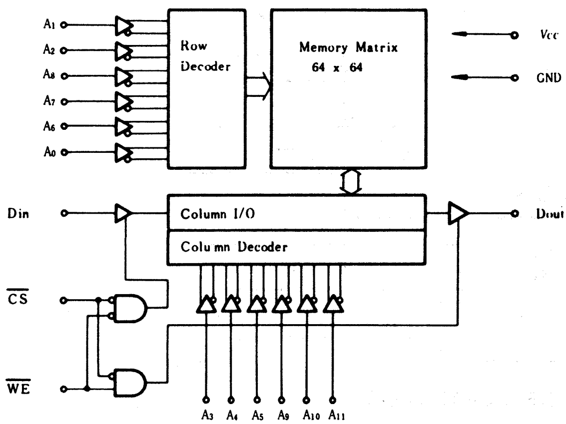
- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 35ns/45ns Max.
- Low Power Standby and Low Power Operation, Standby; 5μW typ., Operation: 150mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM
- Capable of Battery Back up Operation

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	V_T	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature (under bias)	$T_{stg(bias)}$	−10 to +85	℃
Storage Temperature	T_{stg}	−55 to +125	℃

* V_{IN} min = −0.5V (Pulse width ≦ 20ns)

■RECOMMENDED DC OPERATING CONDITIONS (0℃ ≦ Ta ≦ 70℃)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.0	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

* V_{IL} min = −0.5V (Pulse width ≦ 20ns)

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■DC AND OPERATING CHARACTERISTICS ($0°C \leq Ta \leq 70°C$, $V_{CC}=5V\pm10\%$, GND=0V)

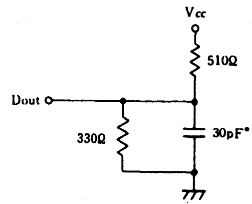
Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.5V$, GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, $V_{out}=0V\sim V_{CC}$	—	—	2	μA
Operating Power Supply Current(1) DC	I_{CC}	$\overline{CS}=V_{IL}$, Output open	—	30	80	mA
Operating Power Supply Current(2) DC	I_{CC1}	$\overline{CS}=V_{IL}$, Minimum Cycle	—	40	80	mA
Standby Power Supply Current(1) DC	I_{SB}	$\overline{CS}=V_{IH}$, V_{CC}=Min to Max	—	5	15	mA
Standby Power Supply Current(2) DC	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{IN}\leq0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	—	1	100	μA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.40	V
Output High Voltage	V_{OH}	$I_{OH}=-4.0mA$	2.4	—	—	V

Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at $V_{CC}=5.0V$, $Ta=25°C$ and specified loading.

■AC TEST CONDITIONS

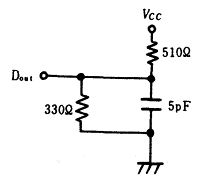
- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels:
  1.5V (HM614HLP-35)
  0.8 to 2.0V (HM614HLP-45)

Output Load A



* Including scope & jig capacitance

Output Load B



■CAPACITANCE ($Ta=25°C$, $f=1.0MHz$)

Item	Symbol	Conditions	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	5	pF
Output Capacitance	C_{out}	$V_{out}=0V$	6	pF

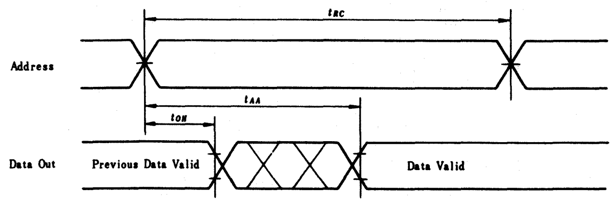
Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS ($Ta=0°C$ to $70°C$, $V_{CC}=5V\pm10\%$, unless otherwise noted.)

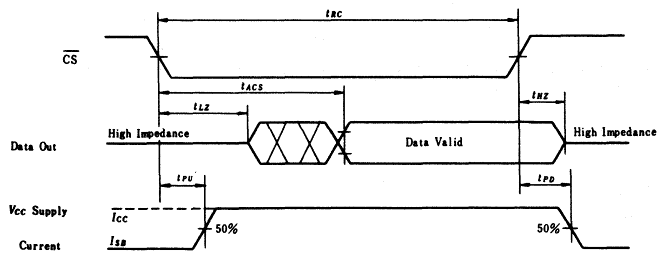
●READ CYCLE

Parameter	Symbol	HM6147HLP-35		HM6147HLP-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	ns	[1]
Address Access Time	t_{AA}	—	35	—	45	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	[2], [3], [7]
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	[2], [3], [7]
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	ns	

● TIMING WAVEFORM OF READ CYCLE NO.1 (4) (5)



● TIMING WAVEFORM OF READ CYCLE NO.2 (4) (6)

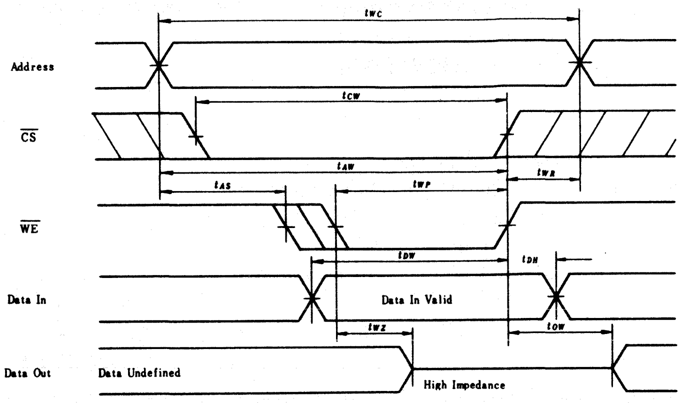


Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitionining address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to divice.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, $\overline{CS}=V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

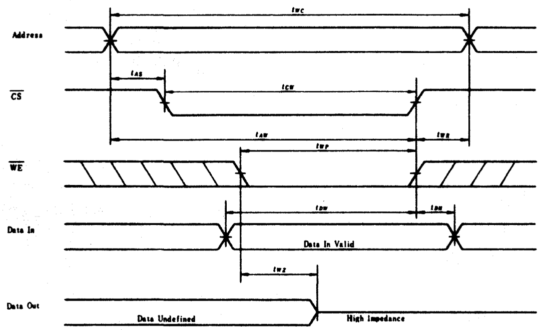
● WRITE CYCLE

Parameter	Symbol	HM6147HLP-35		HM6147HLP-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	ns	(2)
Chip Selection to End of Write	t_{CW}	35	—	45	—	ns	
Address Valid to End of Write	t_{AW}	35	—	45	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{DH}	10	—	10	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	20	0	25	ns	(3), (4)
Output Active from End of Write	t_{OW}	0	—	0	—	ns	(3), (4)

● **TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ CONTROLLED)**



● **TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ CONTROLLED)**



Note) $\overline{CS}$ or $\overline{WE}$ are High for Address Transition

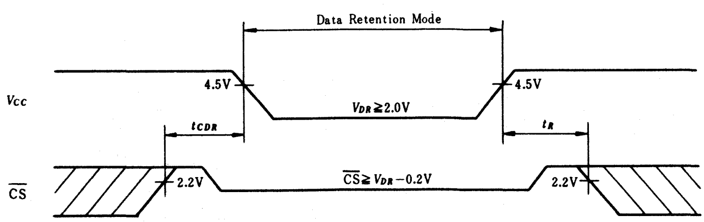
Notes:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0℃ to +70℃)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{CC}=2.0V$, $\overline{CS} \geq 2.8V$ $V_{IN} \geq 2.8V$ or $V_{IN} \leq 0.2V$	—	—	40	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*	—	—	ns

* t_{RC}=Read Cycle Time.

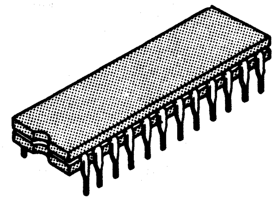
● **LOW V_{CC} DATA RETENTION WAVEFORM**



HM6116-2, HM6116-3, HM6116-4
HM6116P-2, HM6116P-3, HM6116P-4

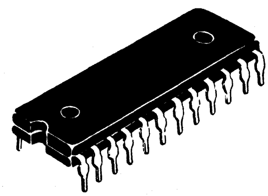
2048-word × 8-bit High Speed Static CMOS RAM

HM6116-2, HM6116-3,
HM6116-4



(DG-24)

HM6116P-2, HM6116P-3,
HM6116P-4

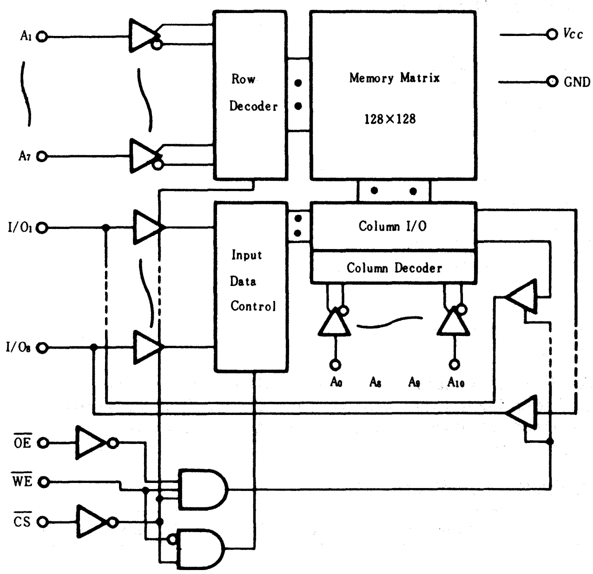


(DP-24)

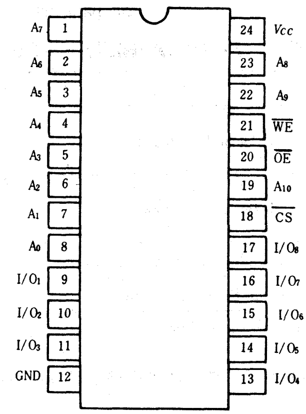
■FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation — Standby: 100μW (typ.) Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature (Plastic)	T_{stg}	−55 to +125	℃
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	℃
Temperature Under Bias	T_{bias}	−10 to +85	℃
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −1.0V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116/P-2			HM6116/P-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	10	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty=100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS}\geqq V_{CC}-0.2$V, $V_{in}\geqq V_{CC}-0.2$V or $V_{in}\leqq 0.2$V	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, Ta=25°C
** Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

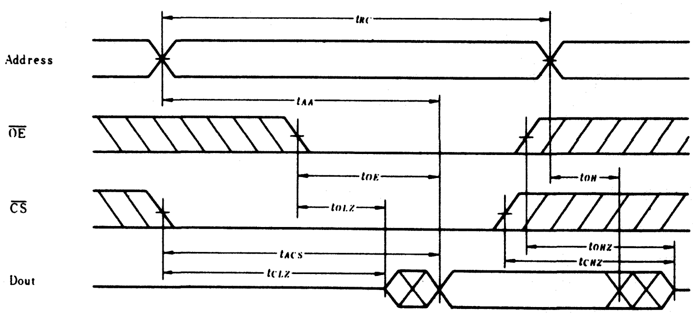
Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

■ CAPACITANCE (f=1MHz, Ta=25°C)

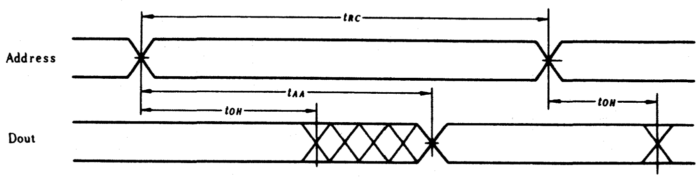
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

■ TIMING WAVEFORM

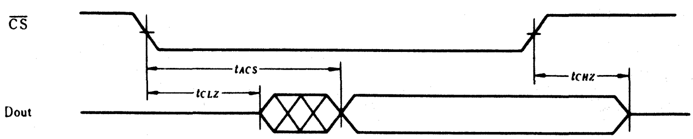
● READ CYCLE (1) (1)(5)



● READ CYCLE (2) (1)(2)(4)(5)

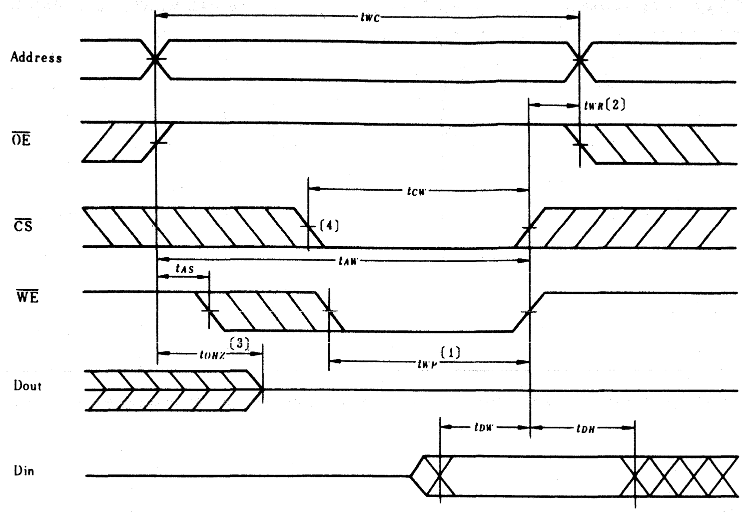


● READ CYCLE (3) (1)(3)(4)(5)

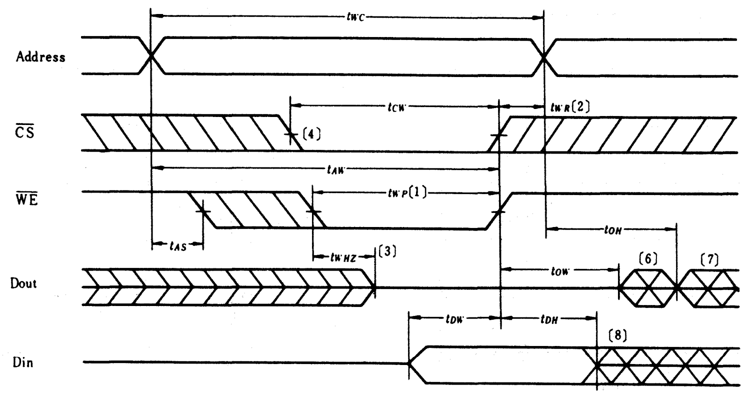


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.
5. When $\overline{CS}$ is Low, the address input must not be in the high impedance state.

WRITE CYCLE (1)

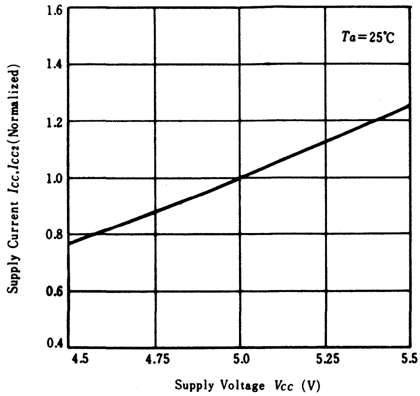


● WRITE CYCLE (2) (5)

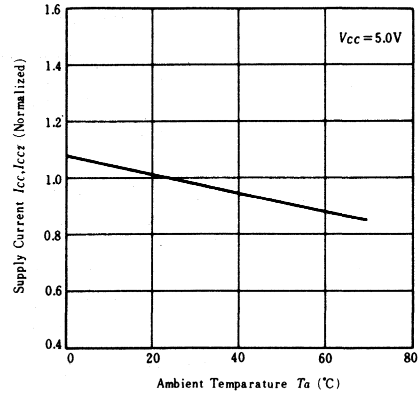


NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

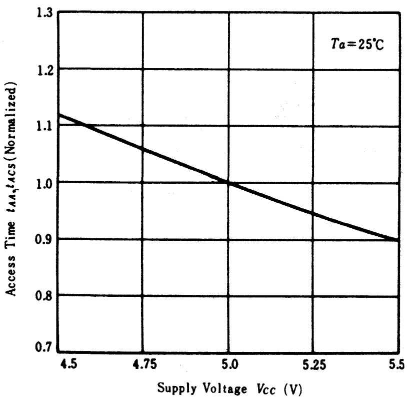
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



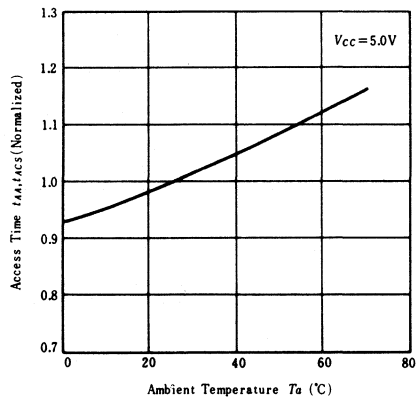
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



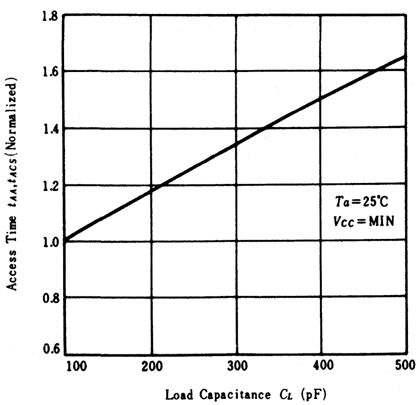
ACCESS TIME
vs. SUPPLY VOLTAGE



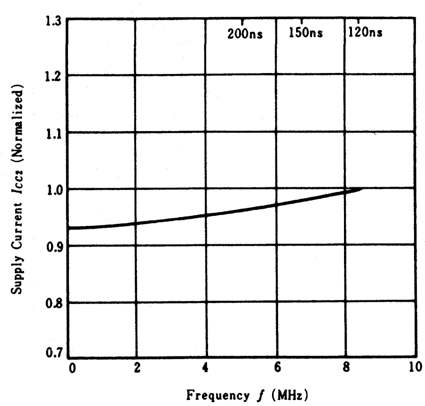
ACCESS TIME
vs. AMBIENT TEMPERATURE



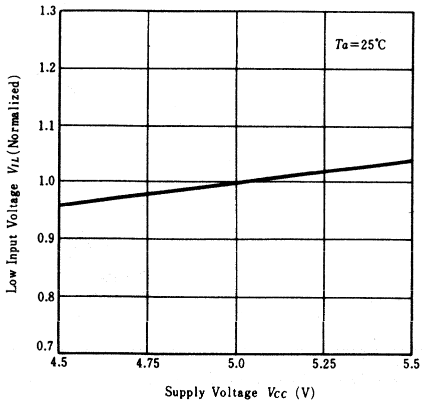
ACCESS TIME
vs. LOAD CAPACITANCE



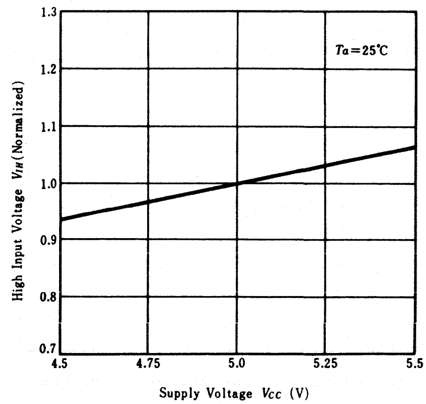
SUPPLY CURRENT
vs. FREQUENCY



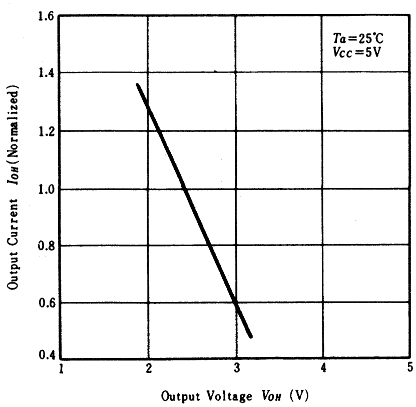
LOW INPUT VOLTAGE
vs. SUPPLY VOLTAGE



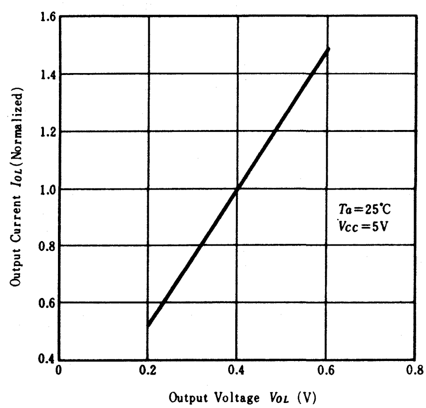
HIGH INPUT VOLTAGE
vs. SUPPLY VOLTAGE



OUTPUT CURRENT
vs. OUTPUT VOLTAGE



OUTPUT CURRENT
vs. OUTPUT VOLTAGE



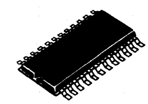
HM6116FP-2, HM6116FP-3, HM6116FP-4

—Preliminary—

2048-word × 8-bit High Speed Static CMOS RAM

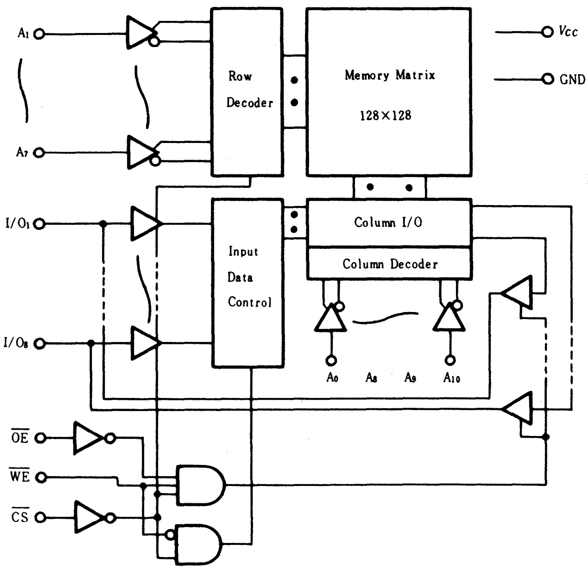
■FEATURES

- High Density Small-Sized Package
- Projection Area Redueced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby Standby: 100μW (typ.)
- Low Power Operation; Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

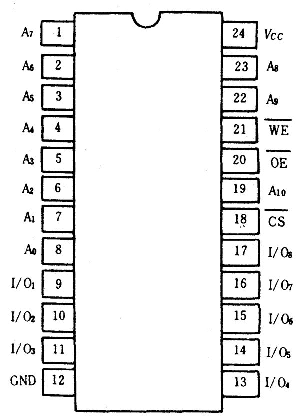


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* V_{IN} min = −1.0V (Pulse Width ≦ 50ns)

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle(1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle(1)
L	L	L	Write	I_{CC}	Din	Write Cycle(2)

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116FP-2			HM6116FP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	10	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty=100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{in}\geq V_{CC}-0.2V$ or $V_{in}\leq 0.2V$	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* V_{CC}=5V, Ta=25°C
** Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116FP-2		HM6116FP-3		HM6116FP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● **WRITE CYCLE**

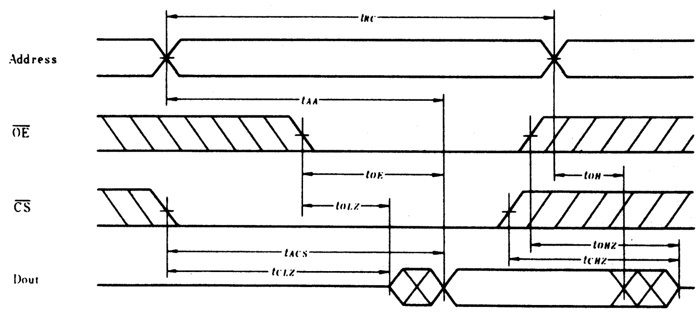
Item	Symbol	HM6116FP-2		HM6116FP-3		HM6116FP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

■ CAPACITANCE (f=1MHz, Ta=25°C)

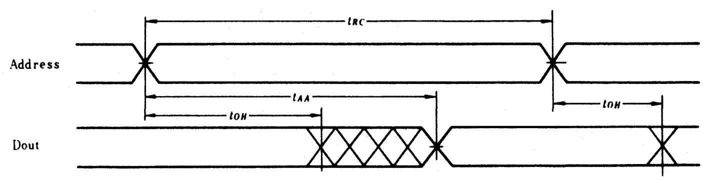
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0V$	5	7	pF

■ TIMING WAVEFORM

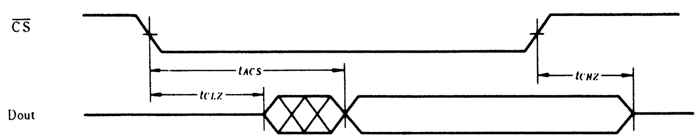
● **READ CYCLE (1)** (1)(5)



● **READ CYCLE (2)** (1)(2)(4)(5)



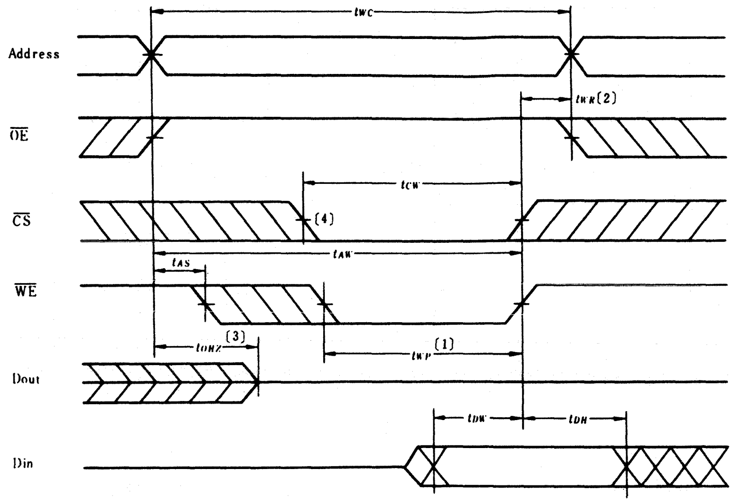
● **READ CYCLE (3)** (1)(3)(4)(5)



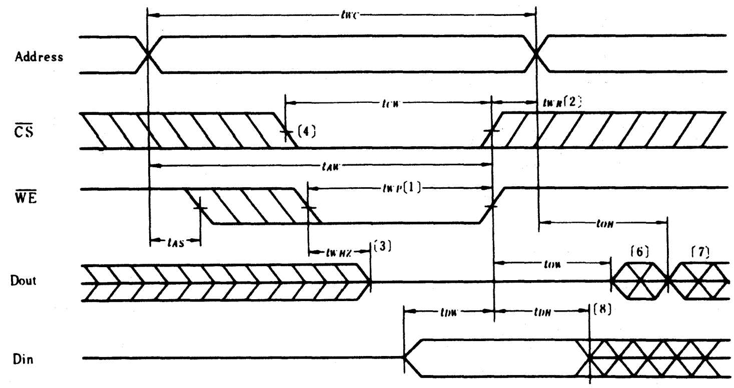
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.
5. When $\overline{CS}$ is Low, the address input must not be in the high impedance state.

■TIMING WAVEFORM

●WRITE CYCLE (1)[1]

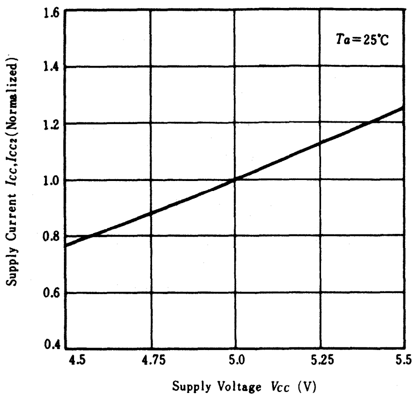


●WRITE CYCLE (2)[5]

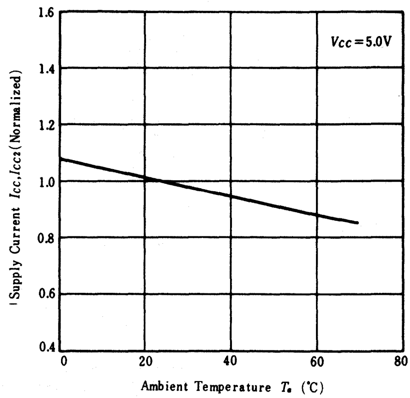


NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

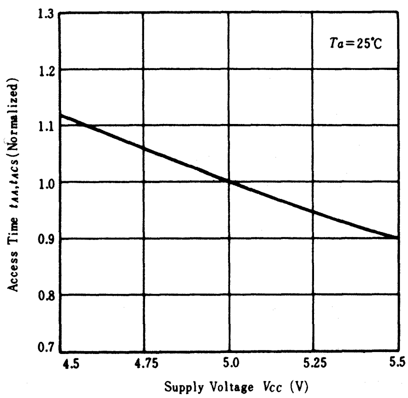
SUPPLY CURRENT vs. SUPPLY VOLTAGE



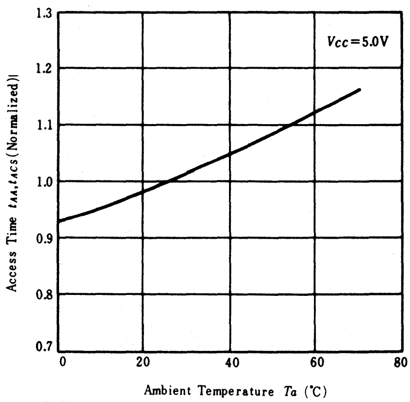
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



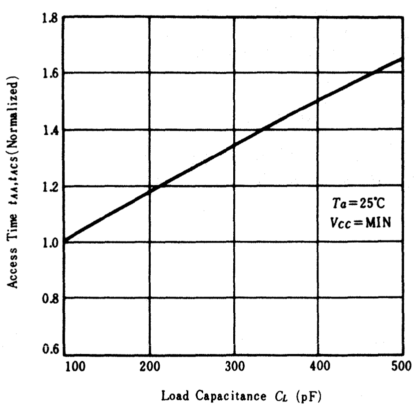
ACCESS TIME vs. SUPPLY VOLTAGE



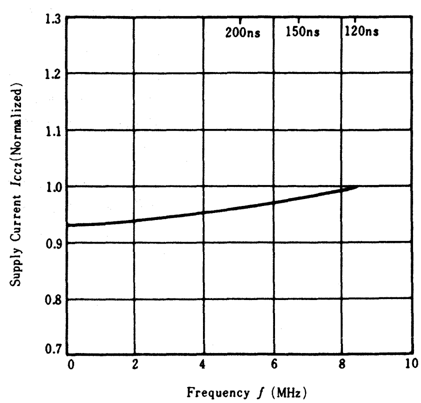
ACCESS TIME vs. AMBIENT TEMPERATURE



ACCESS TIME vs. LOAD CAPACITANCE

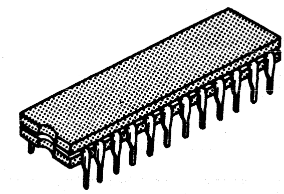


SUPPLY CURRENT vs. FREQUENCY



HM6116L-2, HM6116L-3, HM6116L-4

2048-word×8-bit High Speed Static CMOS RAM

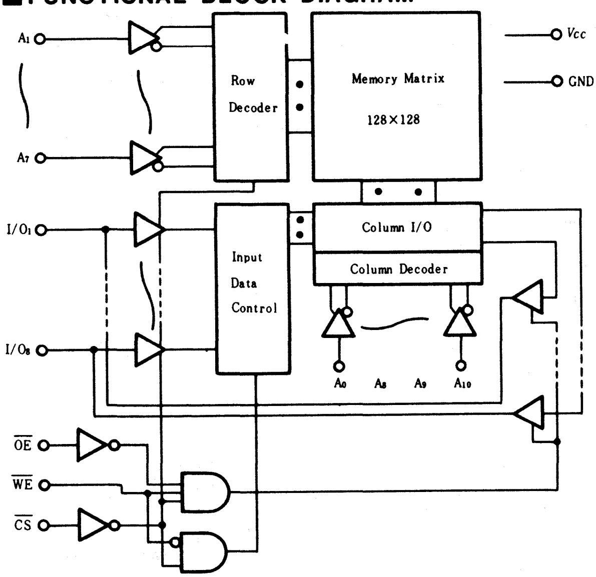


(DG-24)

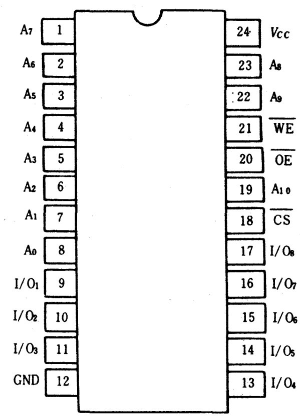
■FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
  Low Power Standby and Standby: 20μW (typ.)
- Low Power Operation; Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −1.0V

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	—	0.8	V

* Pulse Width: 50ns, DC: V_{IL} min = −0.3V

■ DC AND OPERATING CHARACTERISTICS (V_{CC}=5V ±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116L/P-2			HM6116L/P-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	—	30	60	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	min. cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{in}\geq V_{CC}-0.2V$ or $V_{in}\leq 0.2V$	—	4	100	—	4	100	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* : V_{CC}=5V, Ta=25°C
** : Reference Only

■ AC CHARACTERISTICS (V_{CC}=5V ±10%, Ta=0 to +70°C)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116L-2		HM6116L-3		HM6116L-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

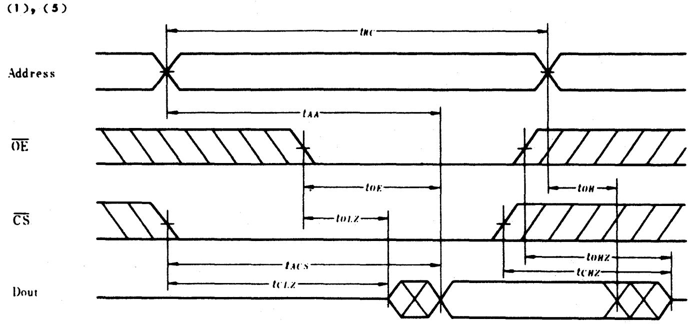
Item	Symbol	HM6116L-2		HM6116L-3		HM6116L-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

■ CAPACITANCE (f=1MHz, Ta=25°C)

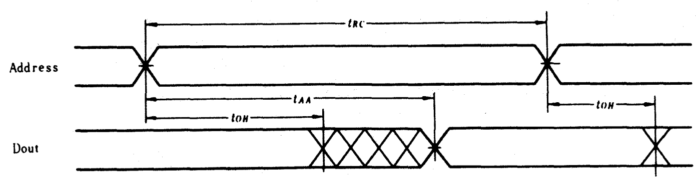
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0V$	5	7	pF

■ TIMING WAVEFORM

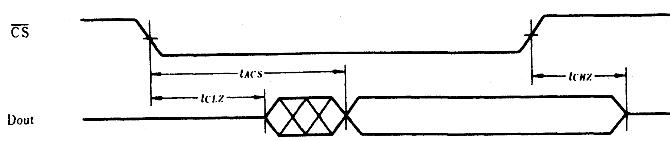
● Read Cycle (1) (1), (5)



● Read Cycle (2) (1), (2), (4), (5)

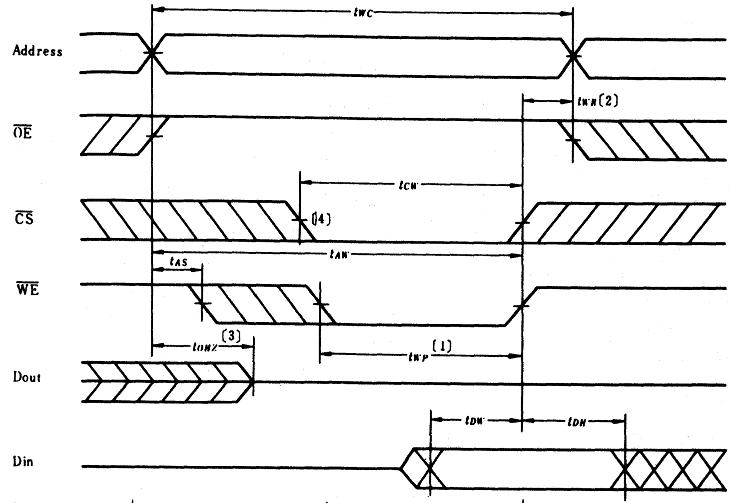


● Read Cycle (3) (1), (3), (4), (5)

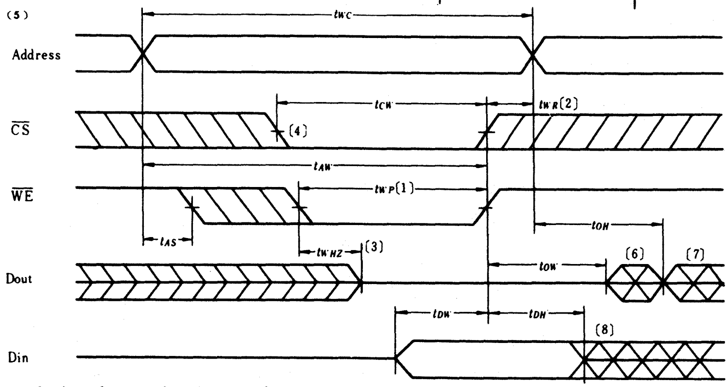


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.
5. When $\overline{CS}$ is Low, the address input must not be in the high impedance state.

● Write Cycle (1)



● Write Cycle (2) (5)



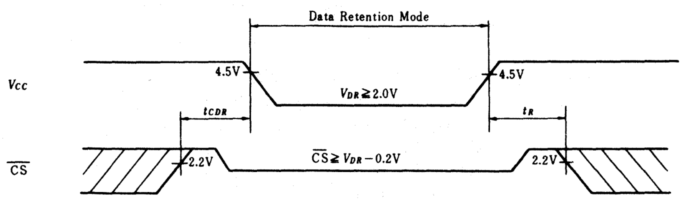
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

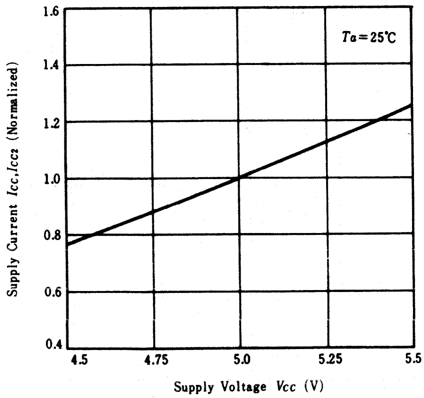
Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*	V_{CC}=3.0V, $\overline{CS} \geq 2.8V$, $V_{in} \geq 2.8V$ or $V_{in} \leq 0.2V$	—	—	50	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

* V_{IL}=−0.3V min.
** t_{RC}=Read Cycle Time.

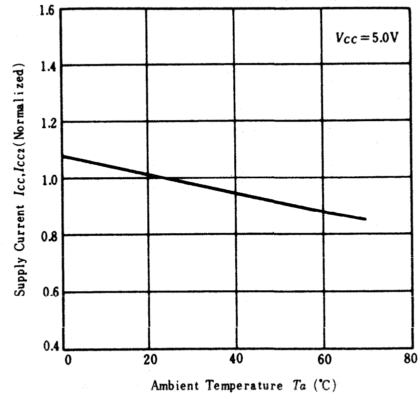
● Low Vcc Data Retention Waveform



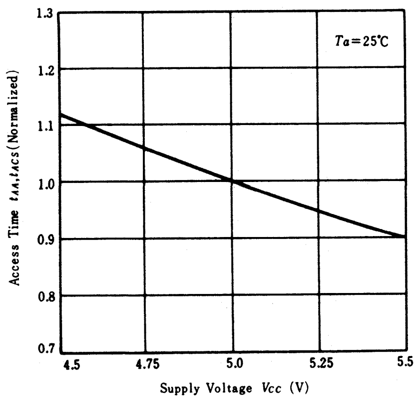
SUPPLY CURRENT vs. SUPPLY VOLTAGE



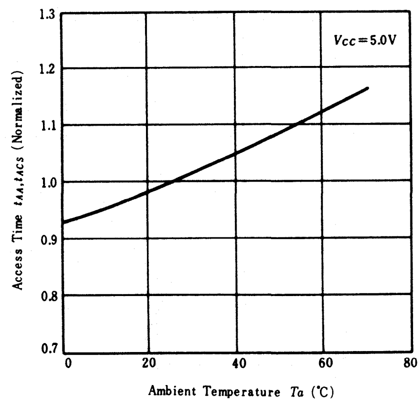
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



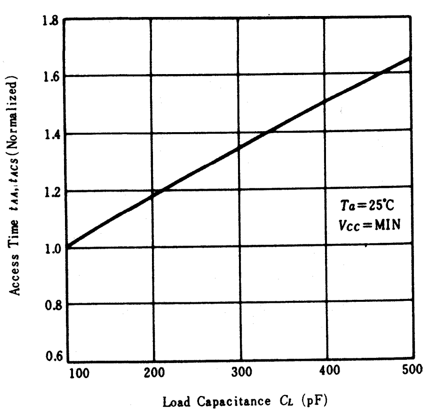
ACCESS TIME vs. SUPPLY VOLTAGE



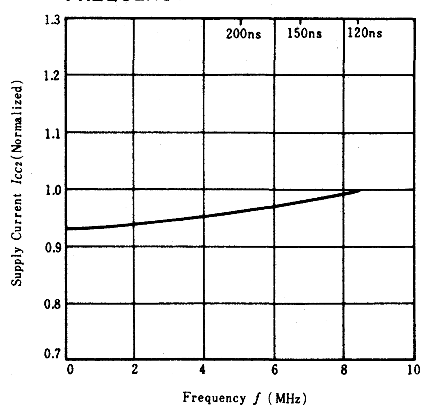
ACCESS TIME vs. AMBIENT TEMPERATURE



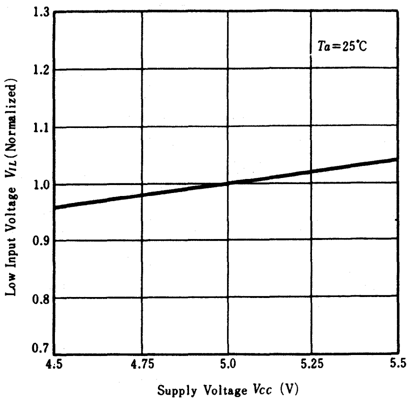
ACCESS TIME vs. LOAD CAPACITANCE



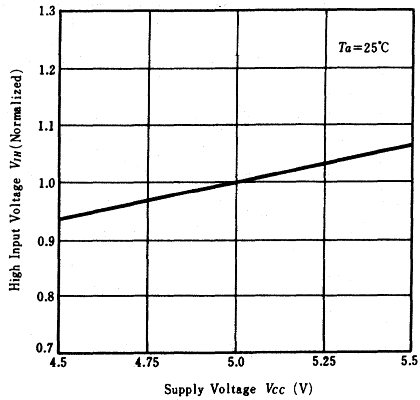
SUPPLY CURRENT vs. FREQUENCY



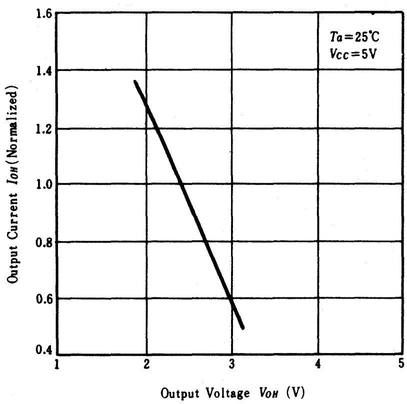
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



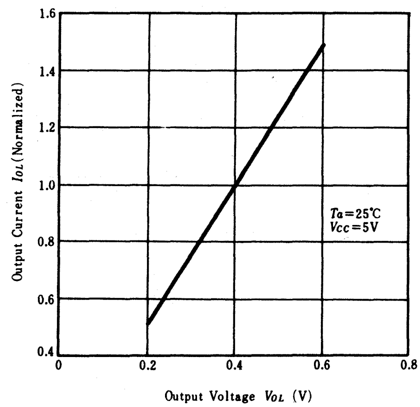
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



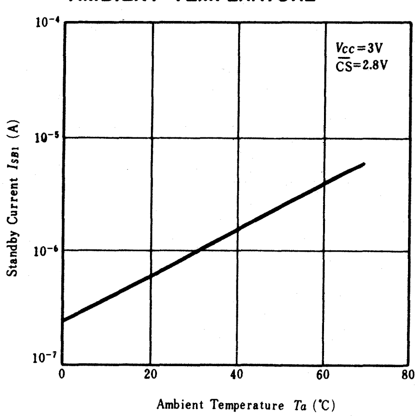
OUTPUT CURRENT vs. OUTPUT VOLTAGE



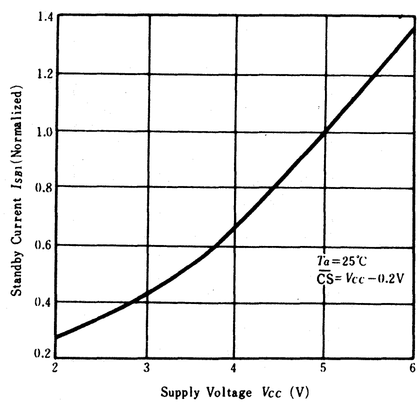
OUTPUT CURRENT vs. OUTPUT VOLTAGE



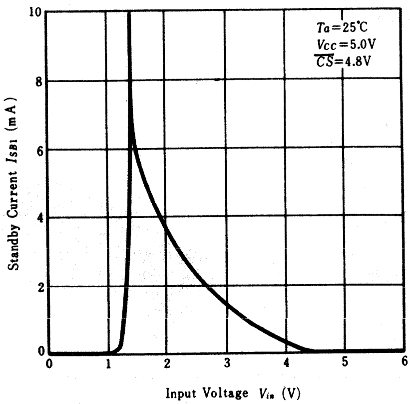
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



STANDBY CURRENT vs. INPUT VOLTAGE

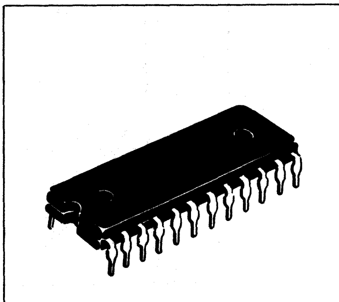


HM6116LP-2, HM6116LP-3, HM6116LP-4

2048-word×8-bit High Speed Static CMOS RAM

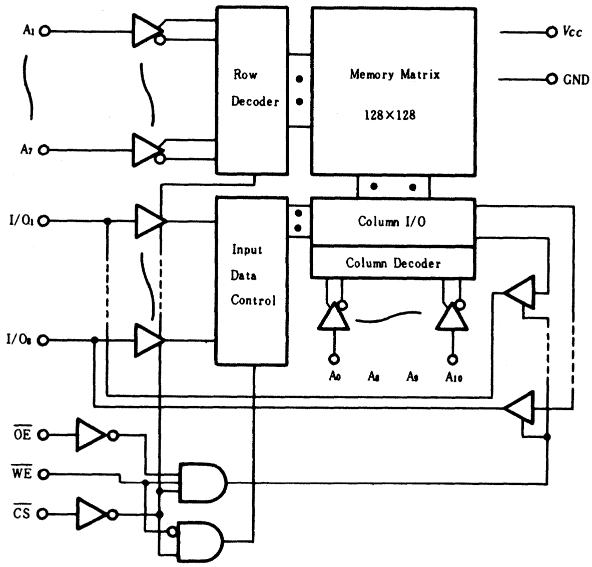
■ FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 10μW (typ.) Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

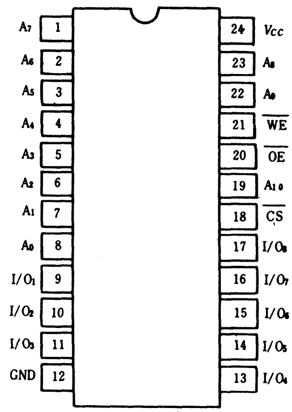


(DP-24)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃
Temperature Under Bias	T_{bias}	−10 to +85	℃
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : −1.0V

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■ RECOMMENDED DC OPERATING CONDITIONS ($Ta=0$ to $+70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	—	0.8	V

* Pulse Width: 50ns, DC: V_{IL} min = −0.3V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, GND=0V, $Ta=0$ to $+70°C$)

Item	Symbol	Test Conditions	HM6116LP-2			HM6116LP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\vert I_{LI} \vert$	$V_{CC}=5.5V$, V_{in}=GND to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$\vert I_{LO} \vert$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	—	35	70	—	30	60	mA
	I_{CC1}**	$V_{IH}=3.5V$, $V_{IL}=0.6V$, $I_{I/O}=0mA$	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	min. cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	—	2	50	—	2	50	μA
Output Voltage	V_{OL}	$I_{OL}=4mA$	—	—	0.4	—	—	—	V
		$I_{OL}=2.1mA$	—	—	—	—	—	0.4	
	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	2.4	—	—	V

* : $V_{CC}=5V$, $Ta=25°C$
** : Reference Only

■ AC CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $Ta=0$ to $+70°C$)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

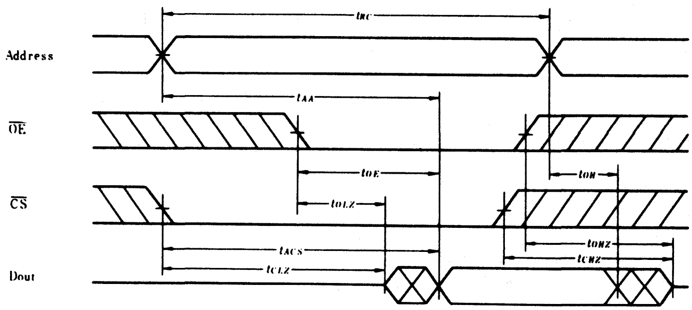
Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

■ CAPACITANCE (f=1MHz, Ta=25°C)

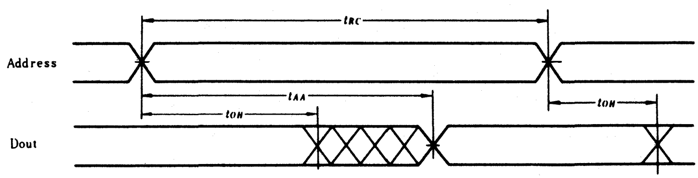
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0V$	5	7	pF

■ TIMING WAVEFORM

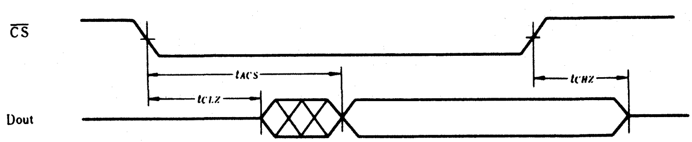
● Read Cycle (1) (1), (5)



● Read Cycle (2) (1), (2), (4), (5)

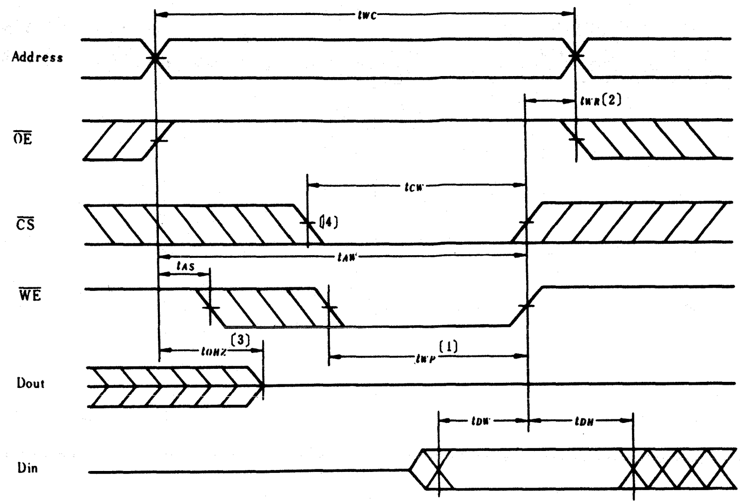


● Read Cycle (3) (1), (3), (4), (5)

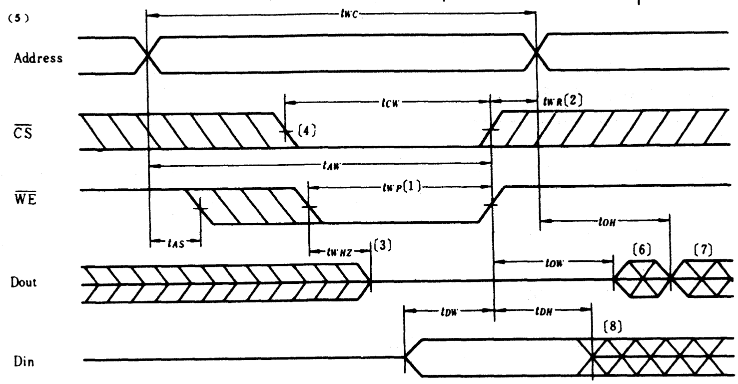


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.
5. When $\overline{CS}$ is Low, the address input must not be in the high impedance state.

● **Write Cycle (1)**



● **Write Cycle (2)** (5)



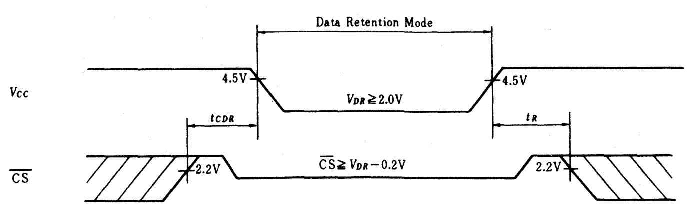
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70°C)

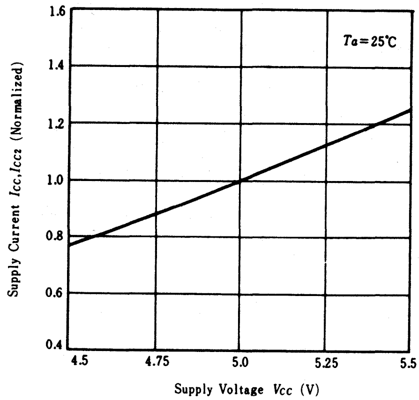
Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{in} \geq V_{CC} - 0.2V$ or $V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*	$V_{CC}=3.0V$, $\overline{CS} \geq 2.8V$, $V_{in} \geq 2.8V$ or $V_{in} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

* 10 μA max at Ta=0°C to +40°C, V_{IL} min = −0.3V
** t_{RC}=Read Cycle Time.

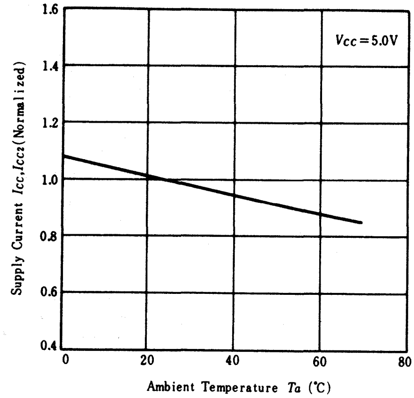
● **Low Vcc Data Retention Waveform**



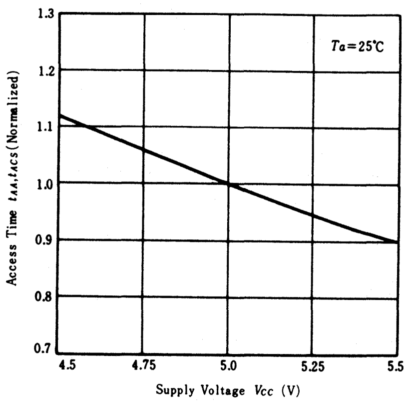
SUPPLY CURRENT vs. SUPPLY VOLTAGE



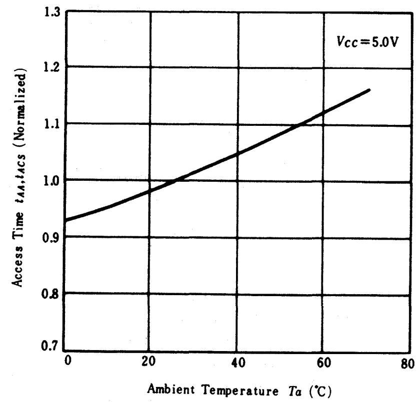
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



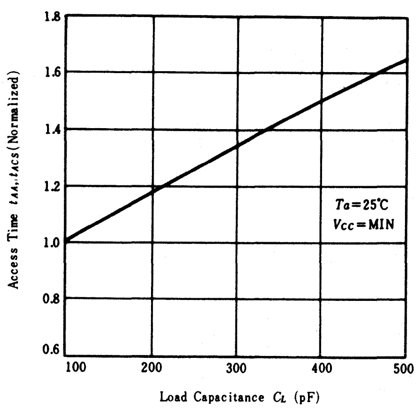
ACCESS TIME vs. SUPPLY VOLTAGE



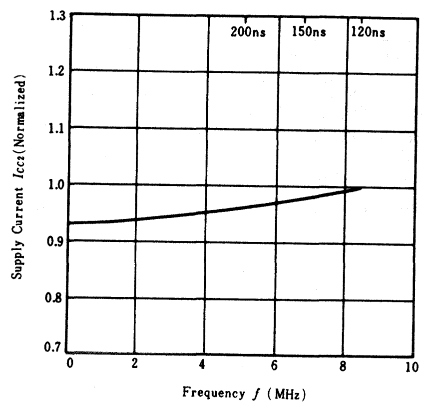
ACCESS TIME vs. AMBIENT TEMPERATURE



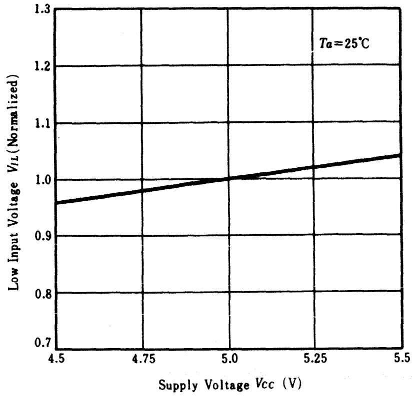
ACCESS TIME vs. LOAD CAPACITANCE



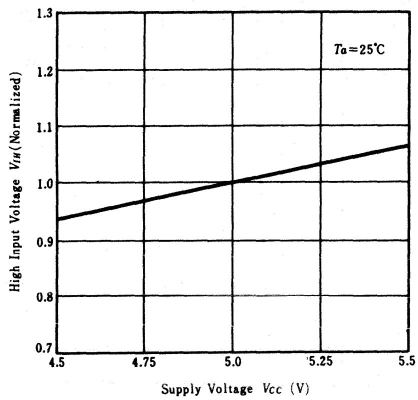
SUPPLY CURRENT vs. FREQUENCY



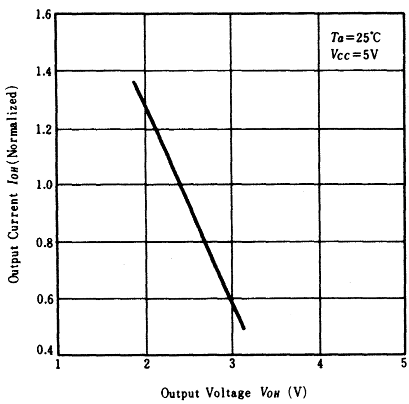
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



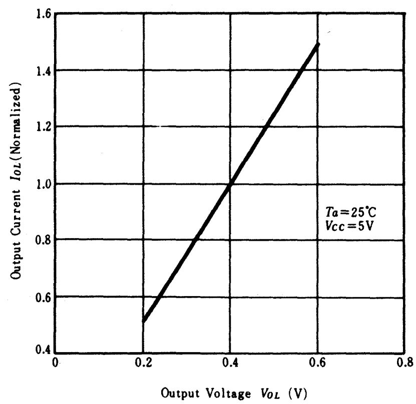
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



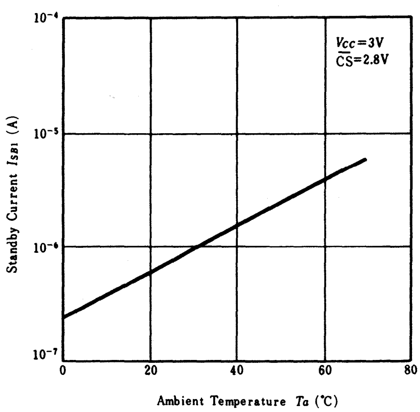
OUTPUT CURRENT vs. OUTPUT VOLTAGE



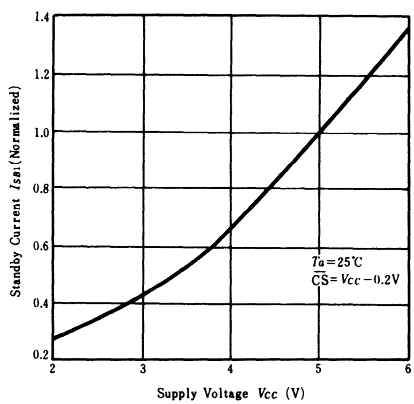
OUTPUT CURRENT vs. OUTPUT VOLTAGE



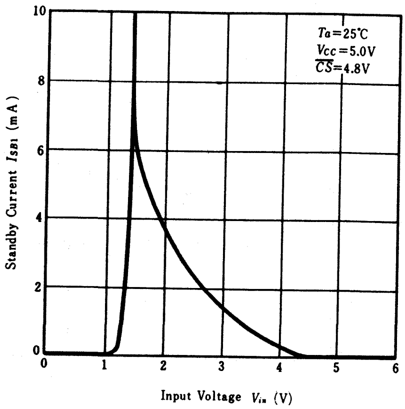
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



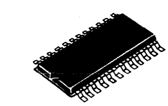
STANDBY CURRENT vs. INPUT VOLTAGE



HM6116LFP-2, HM6116LFP-3, HM6116LFP-4

Preliminary

2048-word × 8-bit High Speed Static CMOS RAM

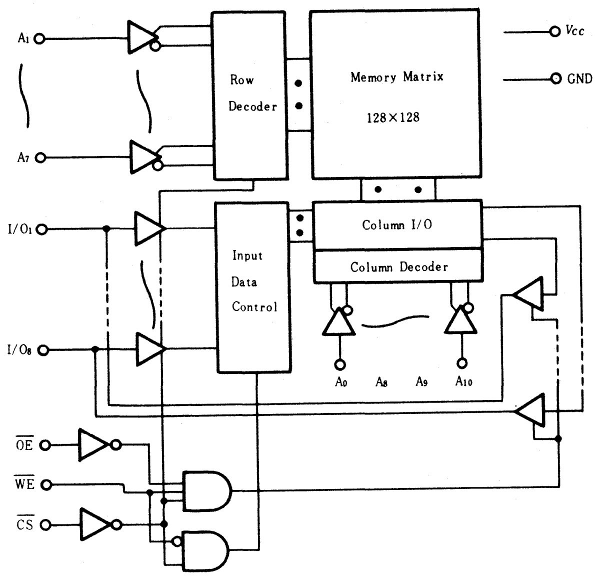


(FP-24)

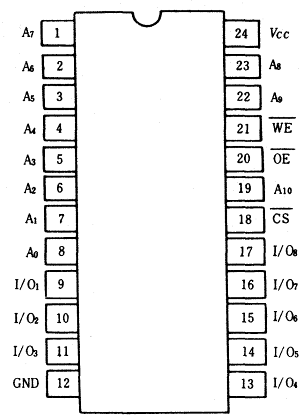
■FEATURES

- High Density Small-sized Package
- Projection Area Redueced to One-Thirds of conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 10μW (typ.) Operation: 160mW (typ.)
- Completely Static RAM: No Clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	−0.5* to +7.0	V
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃
Temperature Under Bias	T_{bias}	−10 to +85	℃
Power Dissipation	P_T	1.0	W

* V_{IN} min = −1.0V (Pulse Width ≦ 50ns)

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. reqarding specifications.

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70℃)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min=−0.3V.

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, GND=0V, Ta=0 to +70℃)

Item	Symbol	Test Conditions	HM6116LFP-2			HM6116LFP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=GND to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Currnnt	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	—	30	60	mA
	I_{CC1}**	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	Min cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2$V, $V_{in} \geqq V_{CC}-0.2$V or $V_{in} \leqq 0.2$V	—	2	50	—	2	50	μA
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* : V_{CC}=5V, Ta=25℃
** : Reference Only

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6116LFP-2		HM6116LFP-3		HM6116LFP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● **WRITE CYCLE**

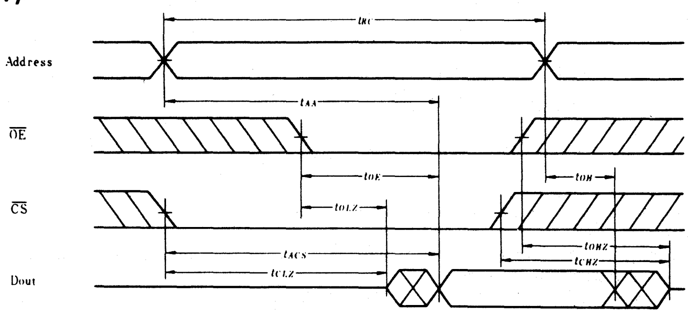
Item	Symbol	HM6116LFP-2		HM6116LFP-3		HM6116LFP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

■ **CAPACITANCE** (f=1MHz, Ta=25°C)

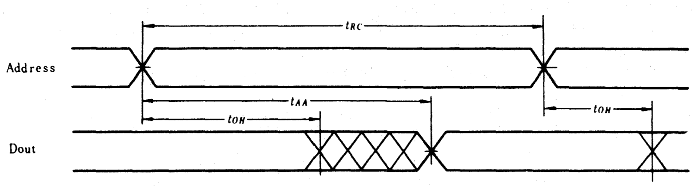
Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	Cin	Vin=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

■ **TIMING WAVEFORM**

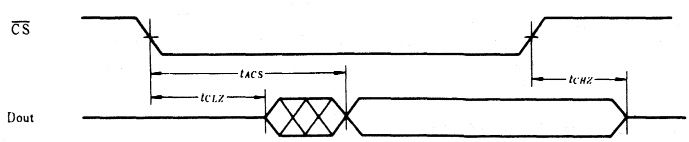
● **READ CYCLE (1)**(1)(5)



● **READ CYCLE (3)**(1)(3)(4)(5)

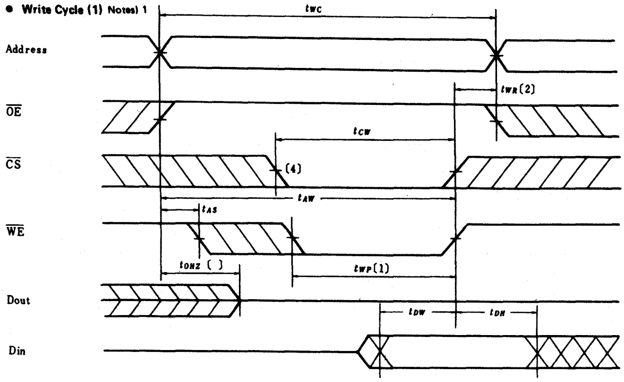


● **READ CYCLE (2)**(1)(2)(4)(5)

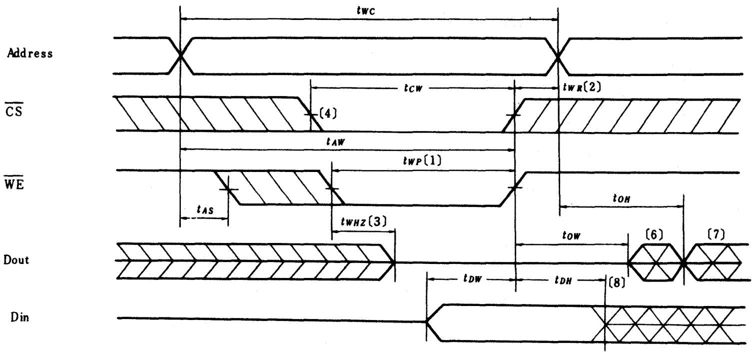


NOTES:
1. $\overline{WE}$ is High for Read Cycle
2. Device is continuously selected, $\overline{CS}$ = V_{IL}
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.
5. When $\overline{CS}$ is Low, the address input must not be in the high impedance state.

●WRITE CYCLE (1)



●WRITE CYCLE (2)(5)



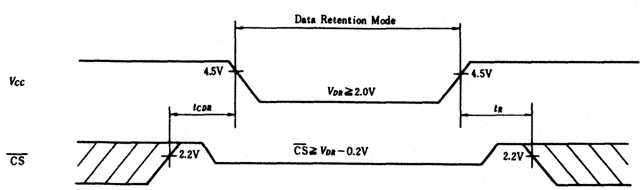
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0 to +70℃)

Item	Symbol	Test Conditions	min	typ	max	Unit
Vcc for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*	$V_{CC}=3.0V$, $\overline{CS} \geqq 2.8V$ $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		**t_{RC}	—	—	ns

* V_{IL} min = −0.3V, 10μA max (at Ta=0 to +40℃)
** t_{RC}=Read Cycle Time.

●Low Vcc DATA RETENTION WAVEFORM

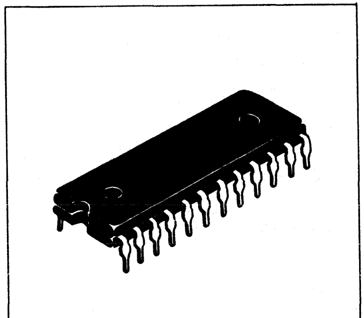


HM6117P-3, HM6117P-4 — Preliminary —

2048-word×8-bit High Speed Static CMOS RAM

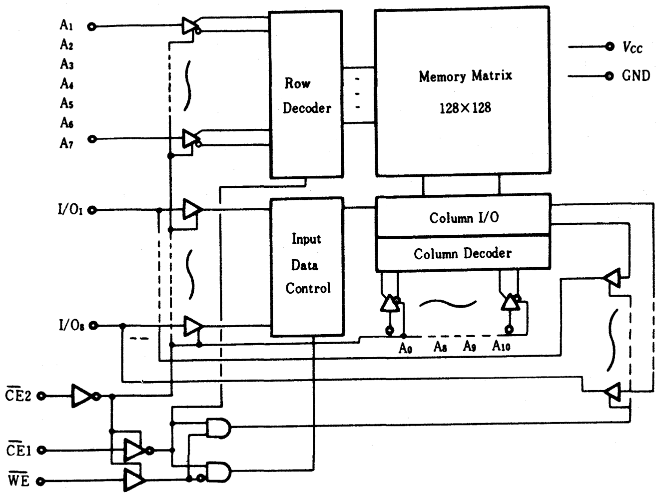
■FEATURES

- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Low Power Operation: Standby: 100μW (typ.) Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

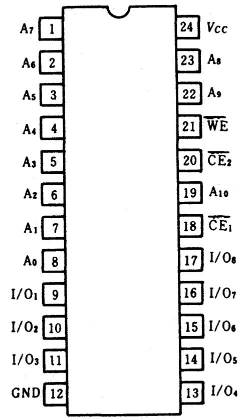


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃
Temperature Under Bias	T_{bias}	−10 to +85	℃

* Pulse width 50ns : −1.0V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq Ta \leq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−1.0*	—	0.8	V

* Pulse width: 50ns, DC: $V_{IL\min} = -0.3V$

■DC AND OPERATING CHARACTERISTICS ($Ta = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, GND = 0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{in} = GND to V_{CC}	—	—	10	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1} = V_{IH}$ or $\overline{CE_2} = V_{IH}$ $V_{I/O}$ = GND to V_{CC}	—	—	10	μA
Operating Power Supply Current: DC	I_{CC}	$\overline{CE_1} = \overline{CE_2} = V_{IL}$, $I_{I/O} = 0mA$	—	40	80	mA
Average Operating Current	I_{CC1}	Min cycle, duty = 100% $\overline{CE_1} = V_{IL}$, $\overline{CE_2} = V_{IL}$	—	40	80	mA
Standby Power Supply Current (1): DC	I_{CCL1}*	$\overline{CE_1} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	0.02	2	mA
Standby Power Supply Current (2): DC	I_{CCL2}*	$\overline{CE_2} \geq V_{CC} - 0.2V$	—	0.02	2	mA
Output low Voltage	V_{OL}	$I_{OL} = 2.1mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -1.0mA$	2.4	—	—	V

Notes: 1) Typical limits are at $V_{CC} = 5.0V$, $Ta = +25°C$
2) *: $V_{IL\min} = -0.3V$

■CAPACITANCE ($Ta = 25°C$, $f = 1.0MHz$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS ($Ta = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise noted)

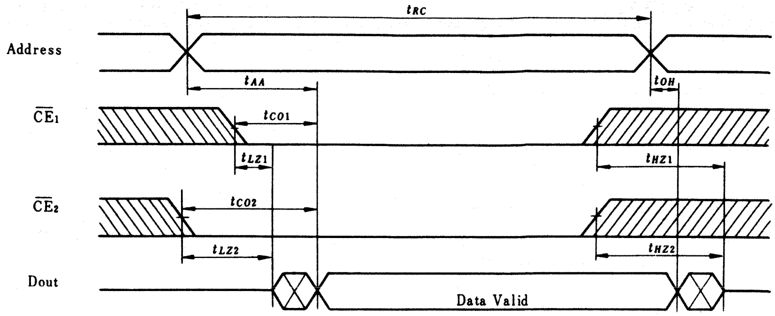
●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1 TTL Gate and C_L=100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1, 2)

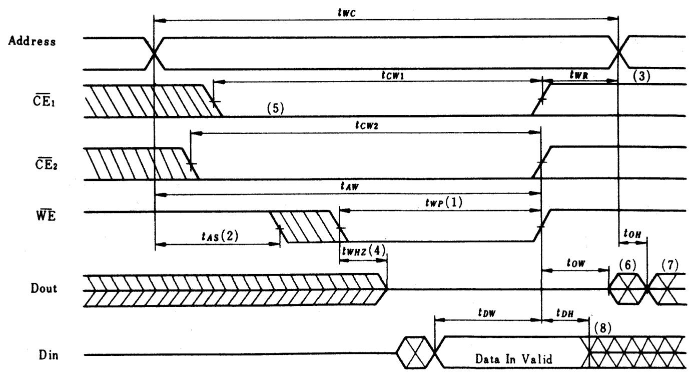


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. When $\overline{CE1}$ and $\overline{CE2}$ are Low, the address input must not be in the high impedance state.

● WRITE CYCLE

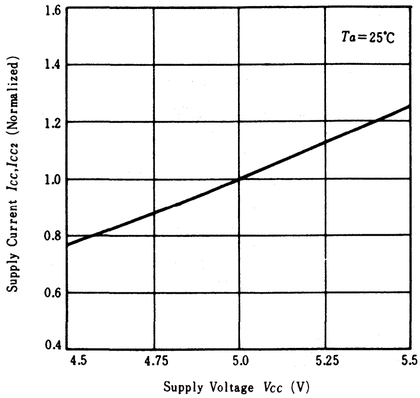
Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE_1}$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE_2}$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE

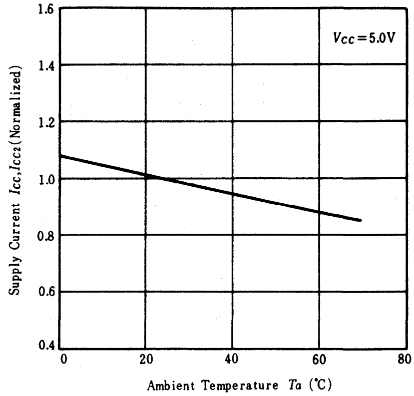


NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{WE}$.
2. t_{AS} is measured from the address changes to the beginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or $\overline{WE}$ going high to the end/of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE_1}$ or $\overline{CE_2}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE_1}$ and $\overline{CE_2}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

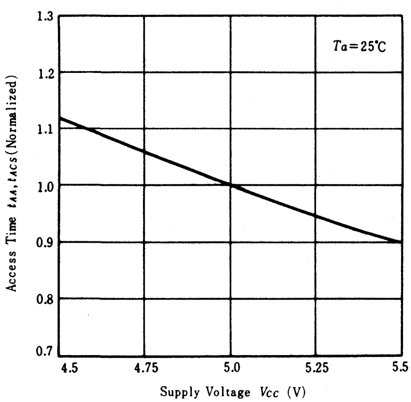
SUPPLY CURRENT vs. SUPPLY VOLTAGE



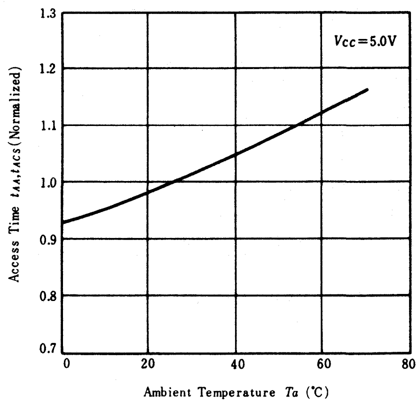
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



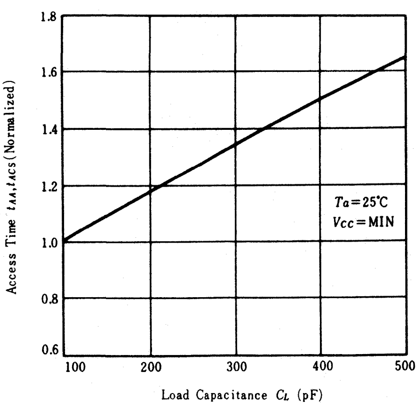
ACCESS TIME vs. SUPPLY VOLTAGE



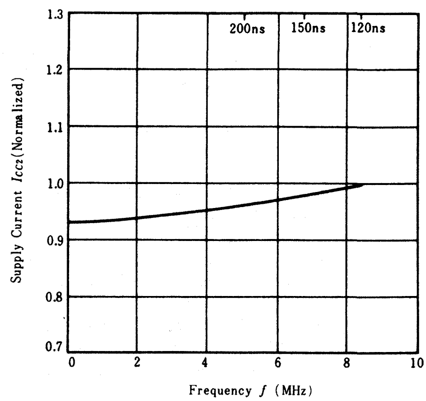
ACCESS TIME vs. AMBIENT TEMPERATURE



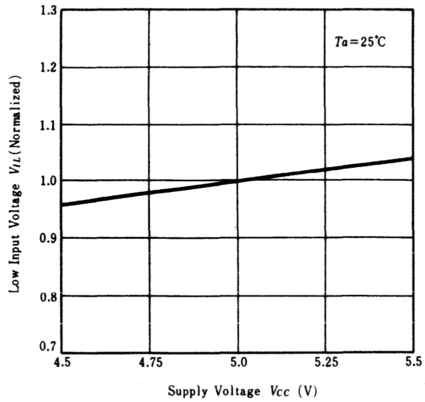
ACCESS TIME vs. LOAD CAPACITANCE



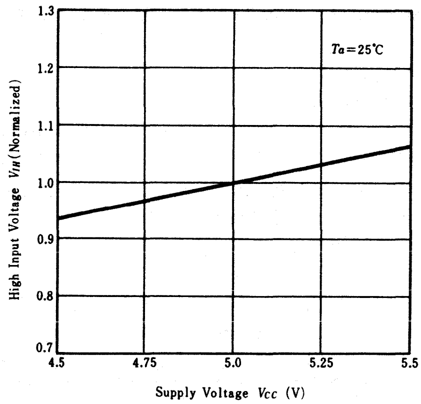
SUPPLY CURRENT vs. FREQUENCY



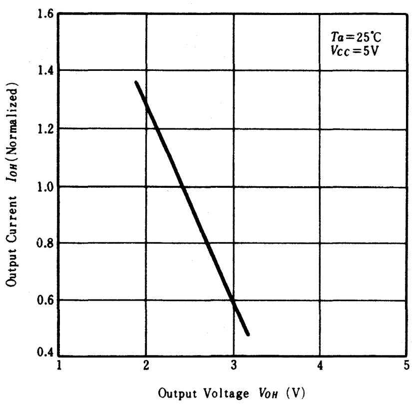
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



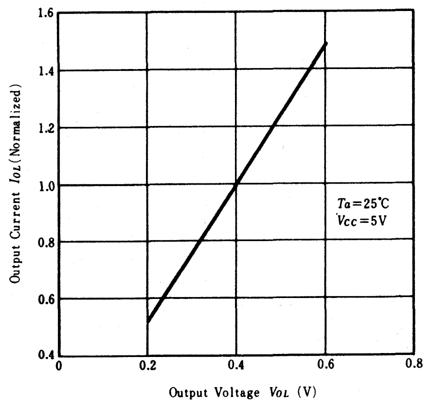
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE

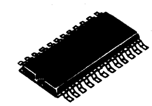


HM6117FP-3, HM6117FP-4 — Preliminary

2048-word × 8-bit High Speed Static CMOS RAM

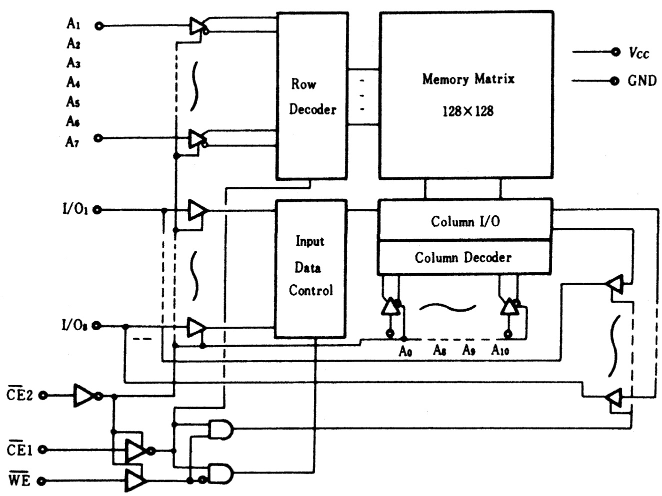
■FEATURES

- High Density Small Sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Standby: 100μW (typ.)
  Low Power Operation: Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

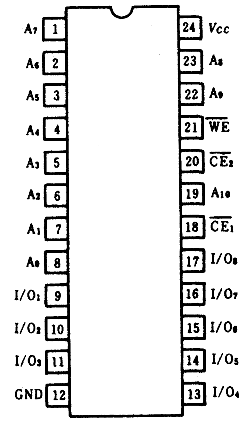


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃
Temperature Under Bias	T_{bias}	−10 to +85	℃

* Pulse width 50ns : −1.0V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■RECOMMENDED DC OPERATING CONDITIONS (0°C≦Ta≦70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage	V_{IL}	−1.0*	—	0.8	V

* Pulse width: 50ns, DC: $V_{IL min}$=−0.3V

■DC AND OPERATING CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{in}=GND to V_{CC}	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE}_1=V_{IH}$ or $\overline{CE}_2=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	10	μA
Operating Power Supply Current: DC	I_{CC}	$\overline{CE}_1=\overline{CE}_2=V_{IL}$, $I_{I/O}$=0mA	—	40	80	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE}_1=V_{IL}$, $\overline{CE}_2=V_{IL}$	—	40	80	mA
Standby Power Supply Current (1): DC	I_{CCL1}*	$\overline{CE}_1 \geqq V_{CC}-0.2V$, $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	—	0.02	2	mA
Standby Power Supply Current (2): DC	I_{CCL2}*	$\overline{CE}_2 \geqq V_{CC}-0.2V$	—	0.02	2	mA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes: 1) Typical limits are at V_{CC}=5.0V, Ta=+25°C
2) *: $V_{IL min}$=−0.3V

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0℃ to +70℃, V_{CC}=5V±10% unless otherwise noted)

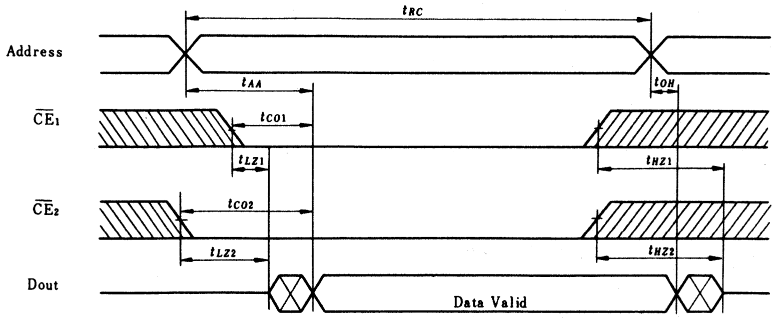
●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

●READ CYCLE

Item	Symbol	HM6117P-3		HM6117P-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE}_1$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE}_2$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE}_1$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE}_2$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE}_1$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE}_2$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

●TIMING WAVEFORM OF READ CYCLE (Notes 1, 2)

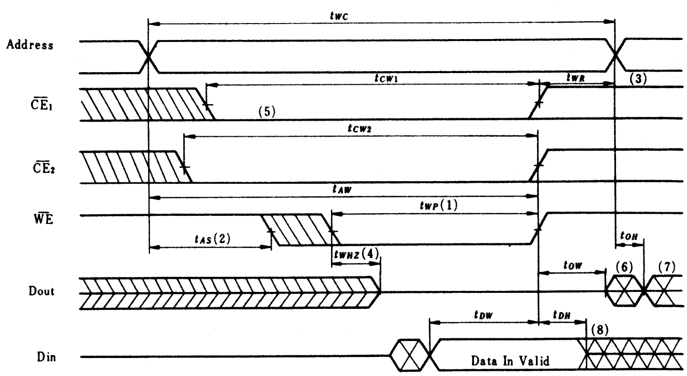


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. When $\overline{CE_1}$ and $\overline{CE_2}$ are Low, the address input must not be in the high impedance state.

●WRITE CYCLE

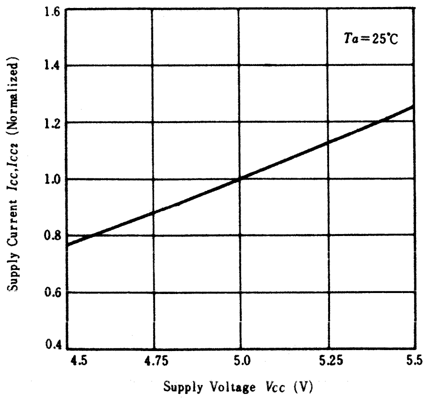
Item	Symbol	HM6117P-3 min	HM6117P-3 max	HM6117P-4 min	HM6117P-4 max	Unit
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE_1}$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE_2}$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

●TIMING WAVEFORM OF WRITE CYCLE

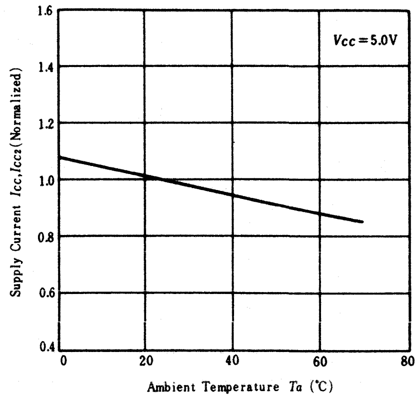


NOTES: 1. A write occurs during the overlap (t_{WP}) of low $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{WE}$.
2. t_{AS} is measured from the address changes to the biginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or $\overline{WE}$ going high to the end/of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE_1}$ or $\overline{CE_2}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE_1}$ and $\overline{CE_2}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

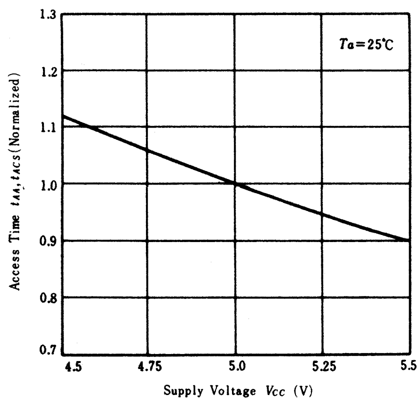
SUPPLY CURRENT vs. SUPPLY VOLTAGE



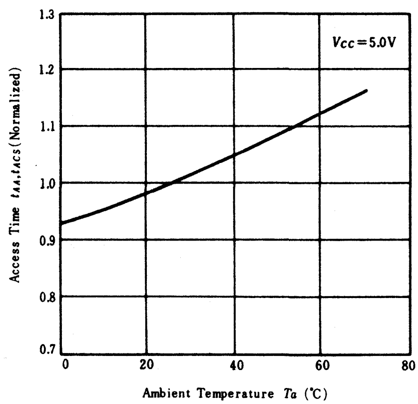
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



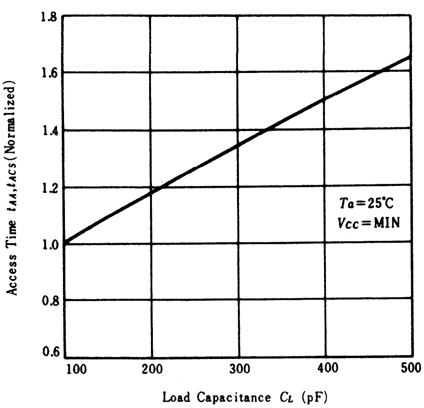
ACCESS TIME vs. SUPPLY VOLTAGE



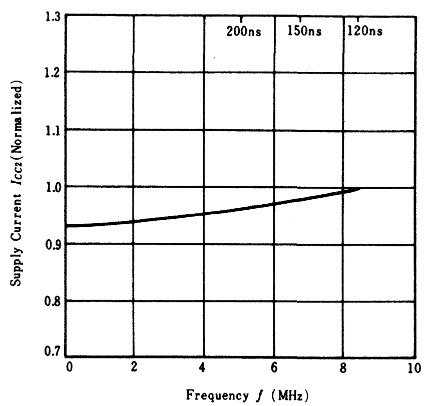
ACCESS TIME vs. AMBIENT TEMPERATURE



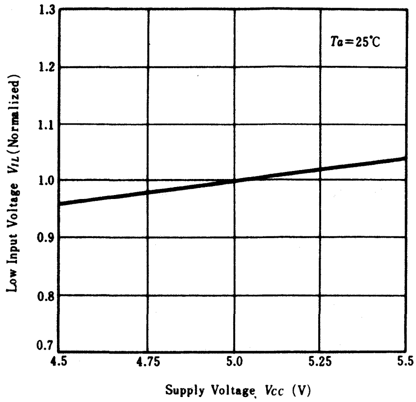
ACCESS TIME vs. LOAD CAPACITANCE



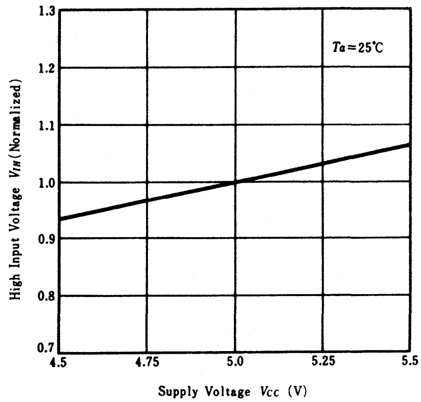
SUPPLY CURRENT vs. FREQUENCY



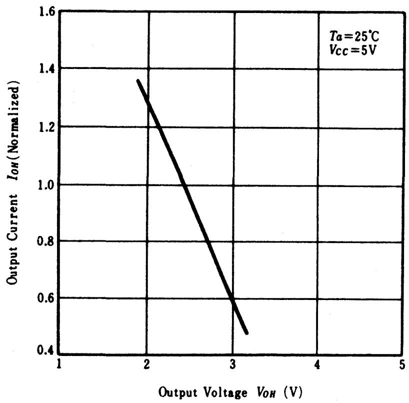
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



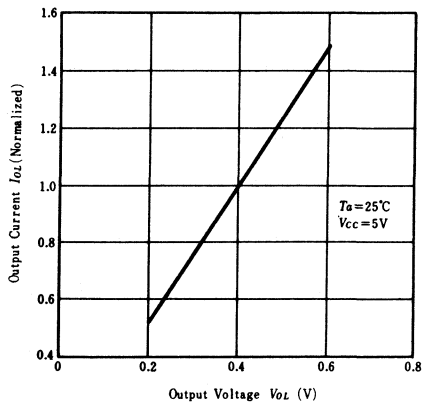
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE

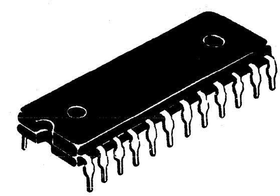


HM6117LP-3, HM6117LP-4 -Preliminary-

2048-word×8-bit High Speed Static CMOS RAM

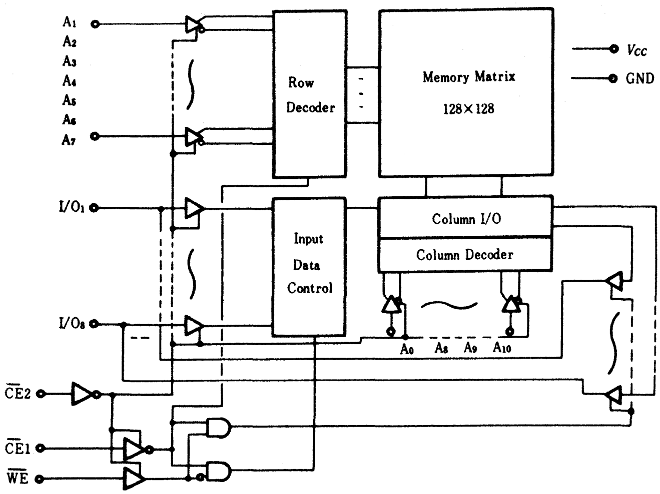
■FEATURES

- Single 5V Supply and High Density 24 Pin Package.
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation;
  Standby: 10μW (typ.) Two Chip Enable Input for Battery Back up
  Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

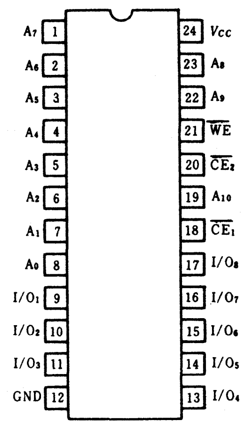


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃
Temperature Under Bias	T_{bias}	−10 to +85	℃
Power Dissipation	P_T	1.0	W

* Pulse width 50ns : −1.0V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to+70°C)

Item		Symbol	min	typ	max	Unit
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
		GND	0	0	0	V
Input High (logic 1) Voltage		V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage		V_{IL}	−1.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{ILmin}=−0.3V.

■DC AND OPERATING CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN}=GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE_1}=V_{IH}$ or $\overline{CE_2}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	2	μA
Operating Power Supply Current : DC	I_{CC}	$\overline{CE_1}=\overline{CE_2}=V_{IL}$, $I_{I/O}$=0mA	—	35	70	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE_1}=V_{IL}$, $\overline{CE_2}=V_{IL}$	—	35	70	mA
Standby Power Supply Current (1) : DC	I_{CCL1}*	$\overline{CE_1} \geq V_{CC}-0.2$V $V_{IN} \geq V_{CC}-0.2$V or $V_{IN} \leq 0.2$V	—	2	50	μA
Standby Power Supply Current (2) : DC	I_{CCL2}*	$\overline{CE_2} \geq V_{CC}-0.2$V	—	2	50	μA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes : 1) Typical limits are at V_{CC}=5.0V, Ta=+25°C
2) * : V_{ILmin}=−0.3V

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note : 1) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10% unless otherwise noted)

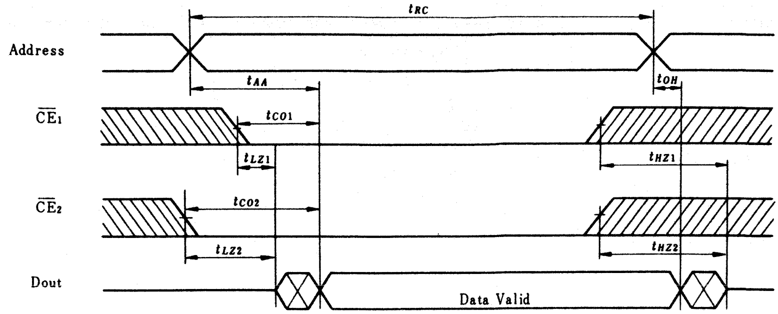
●AC TEST CONDITIONS

Input Pulse Levels .... 0.8V to 2.4V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels ... 1.5V
Output Load .... 1 TTL Gate and C_L = 100pF (Including Scope & Jig)

●READ CYCLE

Item	Symbol	HM6117LP-3		HM6117LP-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE_2}$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE_1}$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE_2}$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE_1}$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE_2}$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1, 2)

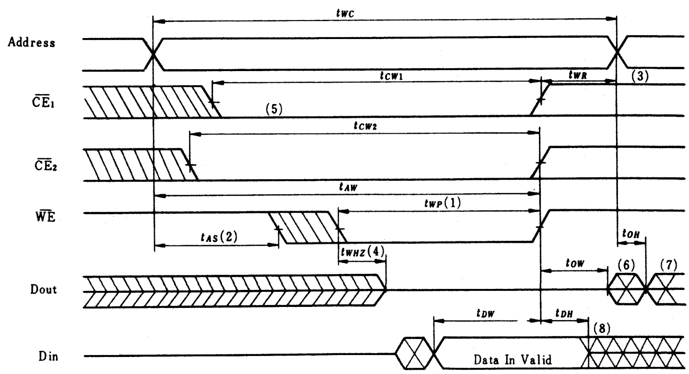


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. When $\overline{CE}_1$ and $\overline{CE}_2$ are low, the address input must not be in the high impedance state.

● WRITE CYCLE

Item	Symbol	HM6117LP-3		HM6117LP-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE}_2$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE



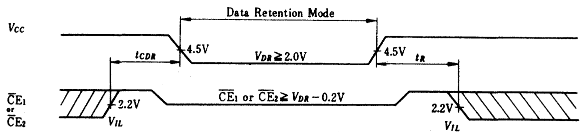
NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$.
2. t_{AS} is measured from the address changes to the bigin-ning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{WE}$ going high to the end/of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}_1$ or $\overline{CE}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE}_1$ and $\overline{CE}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CE_1} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
V_{CC} for Data Retention	V_{DR2}	$\overline{CE_2} \geq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR1}	$V_{CC}=3.0V$, $\overline{CE_1} \geq 2.8V$, $V_{IN} \geq 2.8V$ or $V_{IN} \leq 0.2V$	—	—	30*	μA
Data Retention Current	I_{CCDR2}	$V_{CC}=3.0V$, $\overline{CE_2} \geq V_{CC}-0.2V$	—	—	30*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

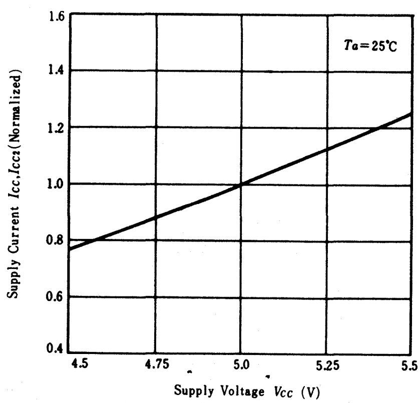
* 10μA max at Ta=0°C to +40°C, V_{IL} min=−0.3V
** t_{RC}=Read Cycle Time

●LOW V_{CC} DATA RETENTION WAVEFORM

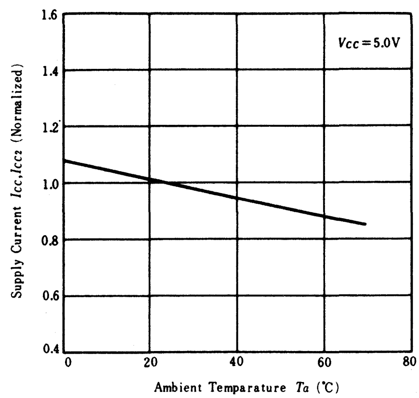


NOTE: 1. $\overline{CE_2}$ controls Address buffer, $\overline{WE}$ buffer, $\overline{CE_1}$ buffer and D_{IN} buffer. If $\overline{CE_2}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_1}$, $D_{I/O}$) can be in the high impedance state. If $\overline{CE_1}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{DE_2}$, $D_{I/O}$) must be $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$.

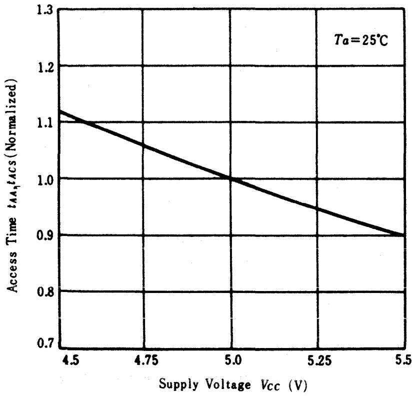
SUPPLY CURRENT vs. SUPPLY VOLTAGE



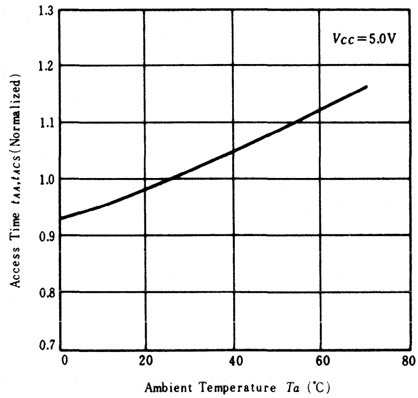
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



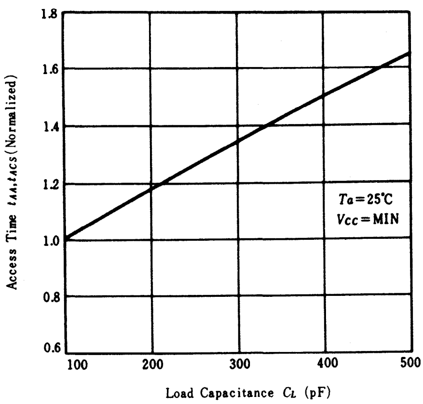
ACCESS TIME vs. SUPPLY VOLTAGE



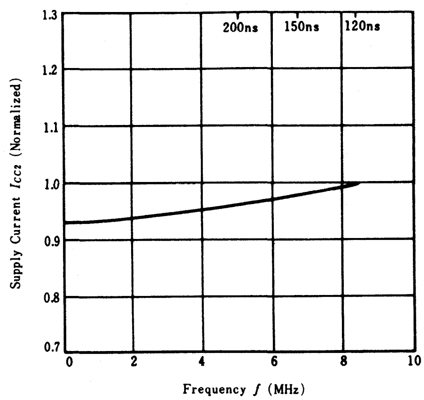
ACCESS TIME vs. AMBIENT TEMPERATURE



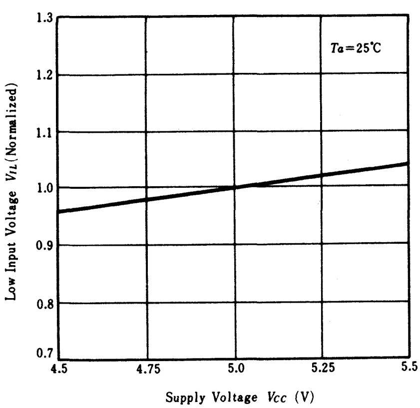
ACCESS TIME vs. LOAD CAPACITANCE



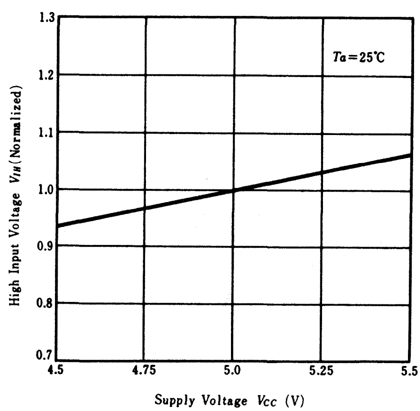
SUPPLY CURRENT vs. FREQUENCY



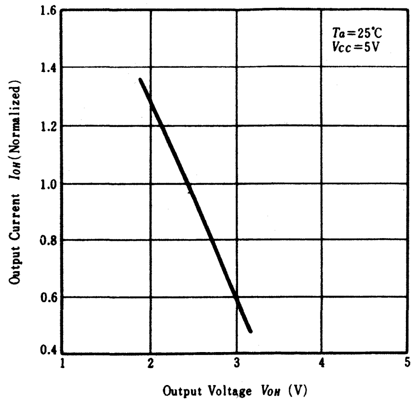
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



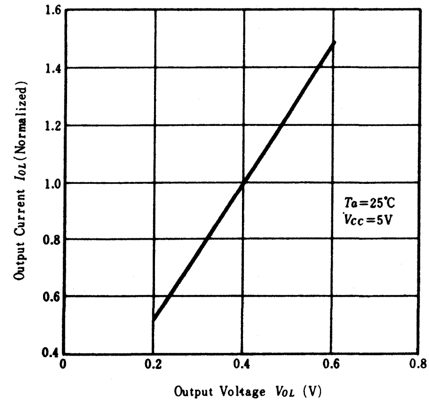
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



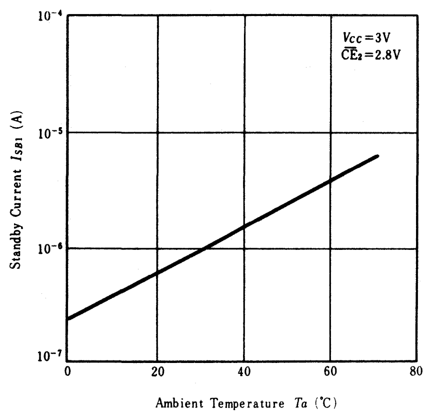
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



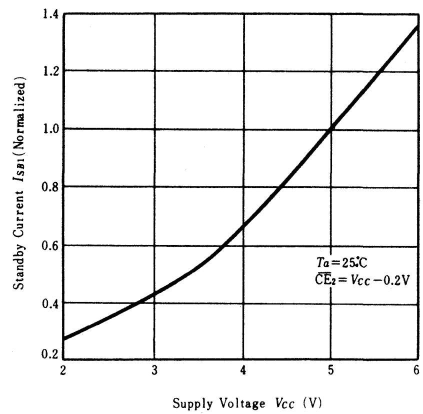
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



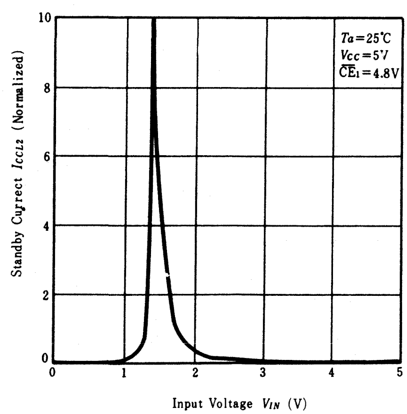
STAND-BY CURRENT vs. AMBIENT TEMPERATURE



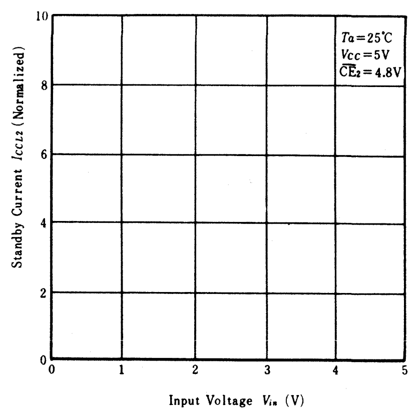
STAND-BY CURRENT vs. SUPPLY VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



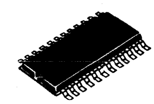
HM6117LFP-3, HM6117LFP-4

Preliminary

2048-word×8-bit High Speed Static CMOS RAM

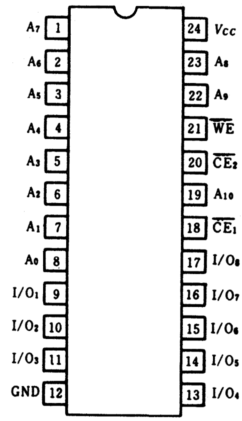
■FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation;
  Standby: 10μW (typ.) Two Chip Enable Input for Battery Back up
  Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation



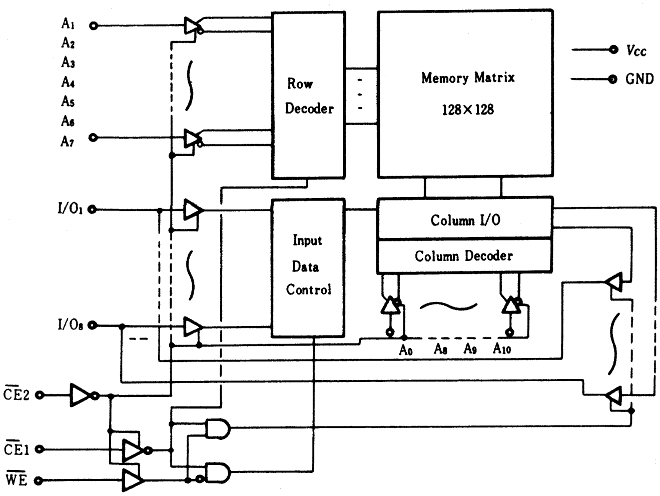
(FP-24)

■PIN ARRANGEMENT



(Top View)

■FUNCTIONAL BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	*−0.5 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃
Temperature Under Bias	T_{bias}	−10 to +85	℃
Power Dissipation	P_T	1.0	W

* Pulse width 50ns : −1.0V

■TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	×	×	Not Selected	I_{CCL1}	High Z
×	H	×	Not Selected	I_{CCL2}	High Z
L	L	H	Read	I_{CC}	Dout
L	L	L	Write	I_{CC}	Din

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0°C to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V
Input low (logic 0) Voltage	V_{IL}	−1.0*	—	0.8	V

* Pulse Width: 50ns, DC: V_{ILmin}=−0.3V.

■DC AND OPERATING CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10%, GND=0V)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{IN}=GND to V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE}_1=V_{IH}$ or $\overline{CE}_2=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	2	μA
Operating Power Supply Current: DC	I_{CC}	$\overline{CE}_1=\overline{CE}_2=V_{IL}$, $I_{I/O}$=0mA	—	35	70	mA
Average Operating Current	I_{CC1}	Min cycle, duty=100% $\overline{CE}_1=V_{IL}$, $\overline{CE}_2=V_{IL}$	—	35	70	mA
Standby Power Supply Current (1): DC	I_{CCL1}*	$\overline{CE}_1 \geqq V_{CC}-0.2V$ $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	—	2	50	μA
Standby Power Supply Current (2): DC	I_{CCL2}*	$\overline{CE}_2 \geqq V_{CC}-0.2V$	—	2	50	μA
Output low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V

Notes: 1) Typical limits are at V_{CC}=5.0V, Ta=+25°C
2) *: V_{ILmin}=−0.3V

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note: 1) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10% unless otherwise noted)

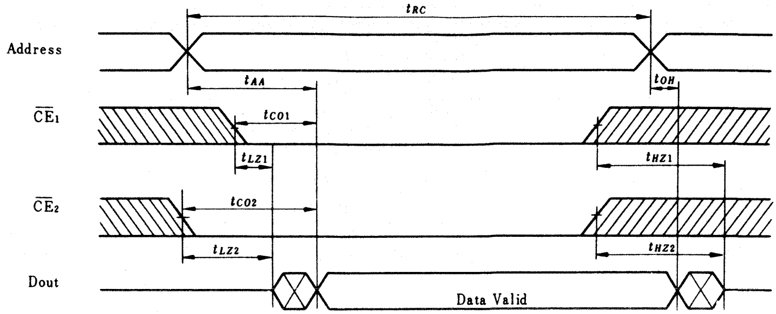
● AC TEST CONDITIONS

Input Pulse Levels .... 0.8V to 2.4V
Input Rise and Fall Times 10ns
Input and Output Timing Reference Levels ... 1.5V
Output Load .... 1 TTL Gate and C_L = 100pF (Including Scope & Jig)

● READ CYCLE

Item	Symbol	HM6117LFP-3		HM6117LFP-4		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	150	—	200	—	ns
Address Access Time	t_{AA}	—	150	—	200	ns
Chip Enable ($\overline{CE}_1$) to Output	t_{CO1}	—	150	—	200	ns
Chip Enable ($\overline{CE}_2$) to Output	t_{CO2}	—	150	—	200	ns
Chip Enable ($\overline{CE}_1$) to Output in Low Z	t_{LZ1}	10	—	10	—	ns
Chip Enable ($\overline{CE}_2$) to Output in Low Z	t_{LZ2}	10	—	10	—	ns
Chip Disable ($\overline{CE}_1$) to Output in High Z	t_{HZ1}	0	70	0	80	ns
Chip Disable ($\overline{CE}_2$) to Output in High Z	t_{HZ2}	0	70	0	80	ns
Output Hold from Address Change	t_{OH}	15	—	15	—	ns

● TIMING WAVEFORM OF READ CYCLE (Notes 1, 2)

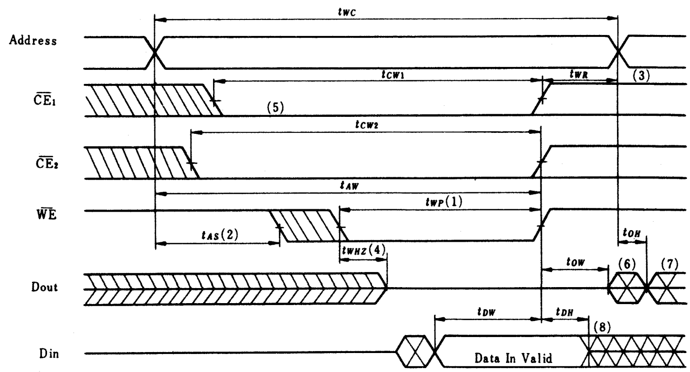


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. When $\overline{CE}_1$ and $\overline{CE}_2$ are low, the address input must be in the high impedance state.

● WRITE CYCLE

Item	Symbol	HM6117LFP-3		HM6117LFP-4		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	150	—	200	—	ns
Chip Enable ($\overline{CE}_1$) to End of Write	t_{CW1}	100	—	120	—	ns
Chip Enable ($\overline{CE}_2$) to End of Write	t_{CW2}	110	—	130	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	ns
Address Valid to End of Write	t_{AW}	130	—	150	—	ns
Write Pulse Width	t_{WP}	100	—	120	—	ns
Write Recovery Time	t_{WR}	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	60	0	70	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	20	—	20	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	ns

● TIMING WAVEFORM OF WRITE CYCLE



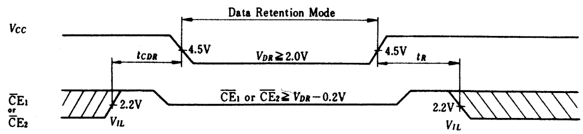
NOTES: 1 A write occurs during the overlap (t_{WP}) of low $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$.
2. t_{AS} is measured from the address changes to the beginning of the write.
3. t_{WR} is measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or $\overline{WE}$ going high to the end/of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}_1$ or $\overline{CE}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transitions, output remain in a high impedance state.
6. Dout is the same phase of write data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CE}_1$ and $\overline{CE}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■LOW V_{CC} DATA RETENTION CHARACTERISTICS (Ta=0°C to +70°C)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CE_1} \geq V_{CC}-0.2V$, $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$	2.0	—	—	V
V_{CC} for Data Retention	V_{DR2}	$\overline{CE_2} \geq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR1}	V_{CC}=3.0V, $\overline{CE_1} \geqq 2.8V$, $V_{IN} \geqq 2.8V$ or $V_{IN} \leqq 0.2V$	—	—	30*	μA
Data Retention Current	I_{CCDR2}	V_{CC}=3.0V, $\overline{CE_2} \geq V_{CC}-0.2V$	—	—	30*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}**	—	—	ns

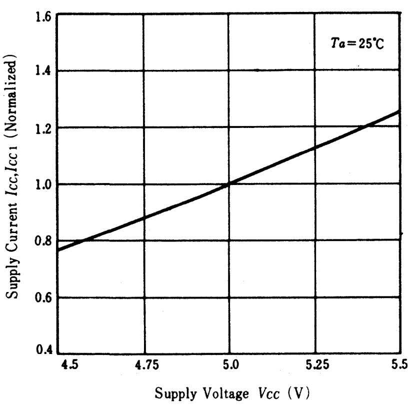
* 10μA max at Ta=0°C to +40°C, V_{IL} min=−0.3V
** t_{RC}=Read Cycle Time

●LOW V_{CC} DATA RETENTION WAVEFORM

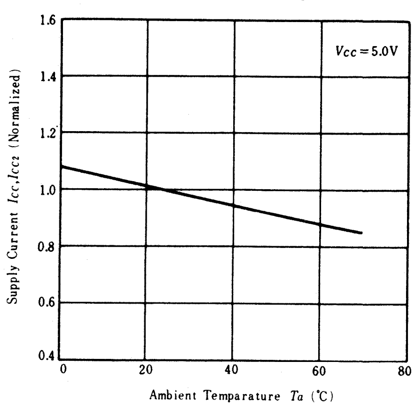


NOTE: 1. $\overline{CE_2}$ controls Address buffer, $\overline{WE}$ buffer, $\overline{CE_1}$ buffer and D_{IN} buffer. If $\overline{CE_2}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_1}$, $D_{I/O}$) can be in the high impedance state. If $\overline{CE_1}$ controls data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CE_2}$, $D_{I/O}$) must be $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$.

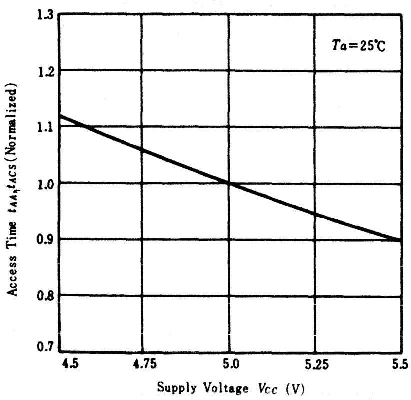
SUPPLY CURRENT vs. SUPPLY VOLTAGE



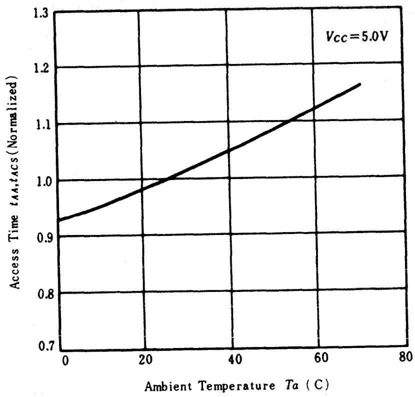
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



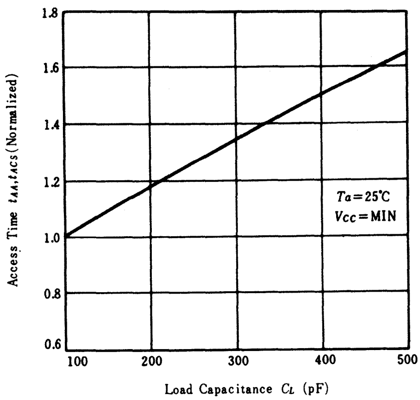
ACCESS TIME vs. SUPPLY VOLTAGE



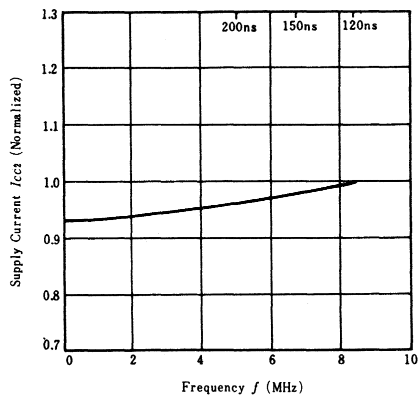
ACCESS TIME vs. AMBIENT TEMPERATURE



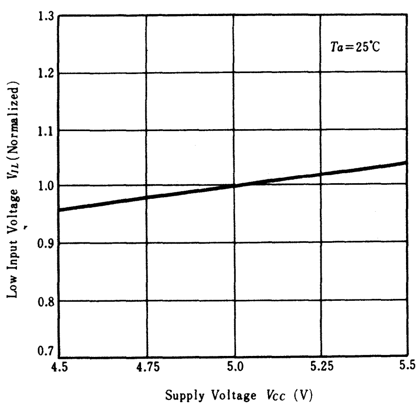
ACCESS TIME vs. LOAD CAPACITANCE



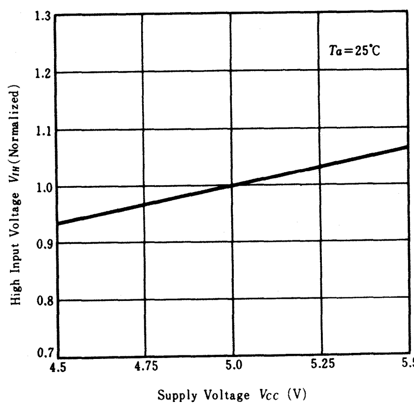
SUPPLY CURRENT vs. FREQUENCY



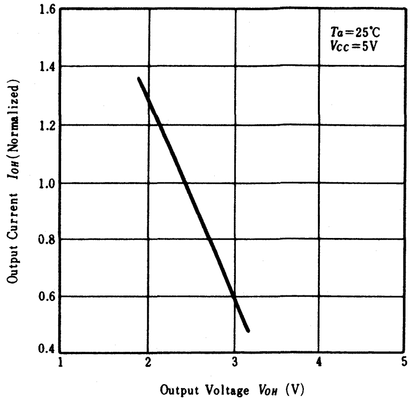
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



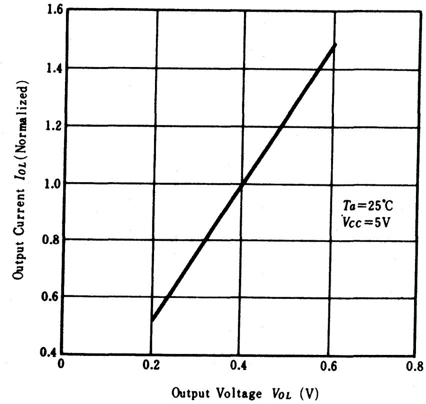
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



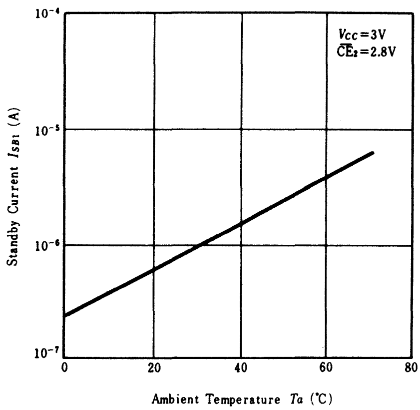
OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



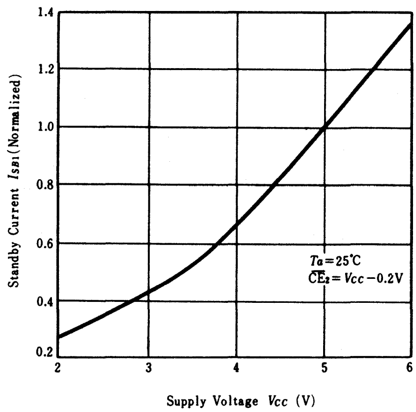
OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



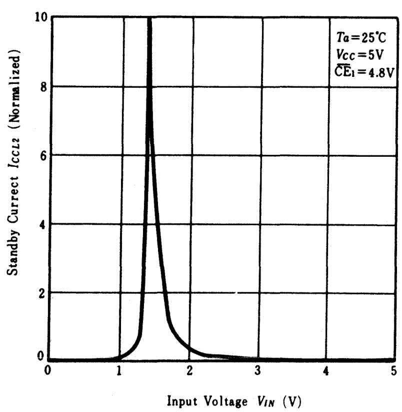
STAND-BY CURRENT vs. AMBIENT TEMPERATURE



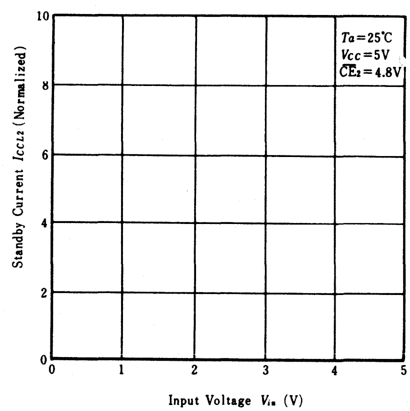
STAND-BY CURRENT vs. SUPPLY VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



STAND-BY CURRENT vs. INPUT VOLTAGE



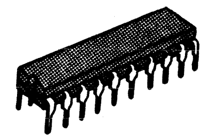
HM6167,HM6167-6,HM6167-8, HM6167P,HM6167P-6,HM6167P-8

16384-word×1-bit High Speed Static CMOS RAM

■FEATURES

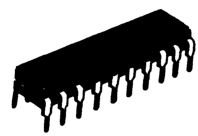
- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time — 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 25mW Typ. and Operating 150mW Typ.
- Completely Static Memory . . . . . No Clock nor Refresh Required
- Fully TTL Compatible — All Inputs and Output
- Separate Data Input and Output . . . . Three State Output
- Pin-Out Compatible with Intel 2167 Series

HM6167, HM6167-6, HM6167-8



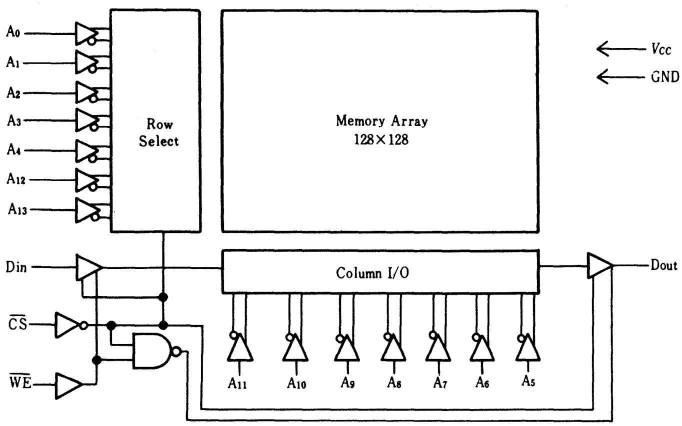
(DG-20)

HM6167P, HM6167P-6, HM6167P-8

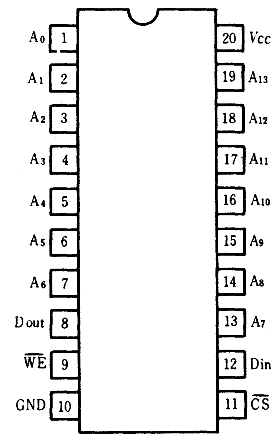


(DP-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature(Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature(Ceramic)	T_{stg}	−65 to +150	°C

■RECOMMENDED DC OPERATING CONDITIONS

(0°C ≦ Ta ≦ 70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−0.5	—	0.8	V

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, Ta=0℃ to +70℃)

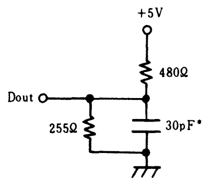
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC}=5.5V$, $V_{IN}=0V \sim V_{CC}$	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, $V_{OUT}=0V \sim V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	20	mA
	I_{SB1}	$\overline{CS}=V_{CC}-0.2V$ $V_{IN} \leqq 0.2V$ or $\geqq V_{CC}-0.2V$	—	0.02	2	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V

Note) Typical limits are at V_{CC}=5.0V, Ta=25℃ and specified loading.

■AC TEST CONDITIONS

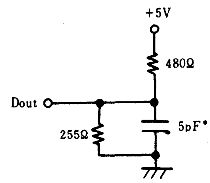
Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



■CAPACITANCE (Ta=25℃, f=1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	$V_{IN}=0V$
Output Capacitance	C_{OUT}	6	pF	$V_{OUT}=0V$

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0℃ to 70℃, unless otherwise noted.)

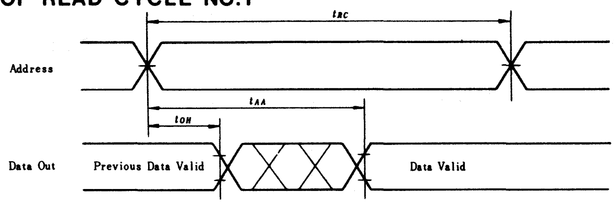
●READ CYCLE

Item	Symbol	HM6167, HM6167P		HM6167-6, HM6167P-6		HM6167-8, HM6167P-8		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	70	—	85	—	100	—	ns
Address Access Time	t_{AA}	—	70	—	85	—	100	ns
Chip Select Access Time	t_{ACS}	—	70	—	85	—	100	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	35	—	40	—	45	ns

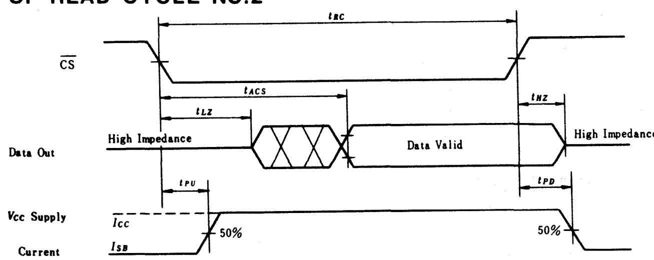
●WRITE CYCLE

Item	Symbol	HM6167, HM6167P		HM6167-6, HM6167P-6		HM6167-8, HM6167P-8		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	70	—	85	—	100	—	ns
Chip Selection to End of Write	t_{CW}	55	—	65	—	80	—	ns
Address Valid to End of Write	t_{AW}	55	—	65	—	80	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	40	—	45	—	55	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	30	—	35	—	40	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}	0	30	0	40	0	40	ns
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns

●TIMING WAVEFORM OF READ CYCLE NO.1 1),2)

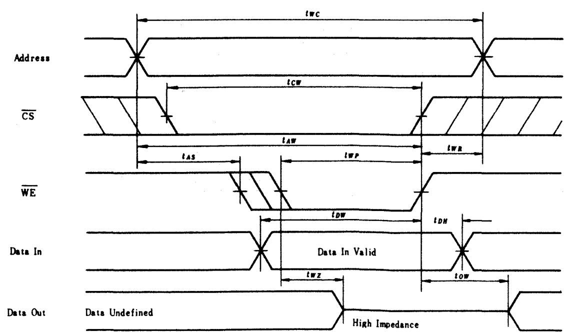


●TIMING WAVEFORM OF READ CYCLE NO.2 1),3)



NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±550mV from steady state voltage with specified loading in Figure B.

●TIMING WAVEFORM OF WRITE CYCLE



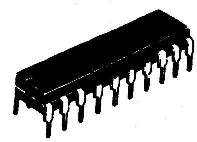
NOTE: 1. Transition is measured ±500mV from steady state voltage with specified loading in Figure B.

HM6167LP, HM6167LP-6, HM6167LP-8

16384-word×1-bit High Speed Static CMOS RAM

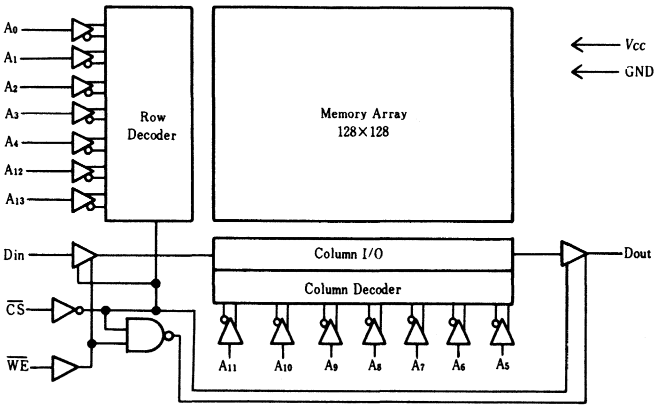
■FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 5μW (typ) and Operating 150mW (typ.)
- Completely Static Memory......No Clock or Refresh Required
- Fully TTL Compatible...............All Inputs and Output
- Separate Data Input and Output ....Three State Output
- Capable of Battery Back up Operation

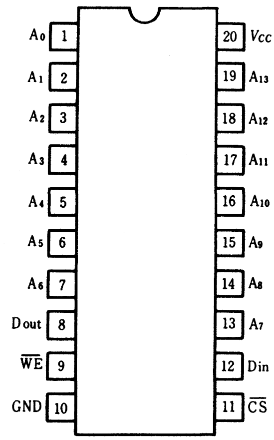


(DP-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	℃
Storage Temperature	T_{stg}	−55 to +125	℃

■RECOMMENDED DC OPERATING CONDITIONS (0℃ ≦ Ta ≦ 70℃)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−0.5	—	0.8	V

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~+70°C)

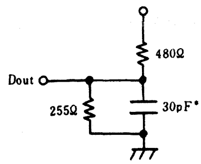
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=5.5V V_{IN}=0V~V_{CC}	—	—	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, V_{out}=0V~V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	20	mA
	I_{SB1}	$\overline{CS}=V_{CC}-0.2V$ $V_{IN}\leqq 0.2V$ or $\geqq V_{CC}-0.2V$	—	1	50	μA
Output Low Voltage	V_{OL}	I_{OL}=8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4mA	2.4	—	—	V

Note) Typical limits are at V_{CC}=5.0V, Ta=25°C and specified loading.

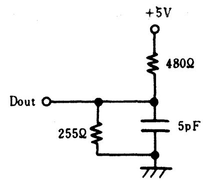
■AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
Input rise and fall times: 5 ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure

Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	6	pF	V_{OUT}=0V

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (Ta=0°C to +70°C, V_{CC}=5V±10%, unless otherwise noted.)

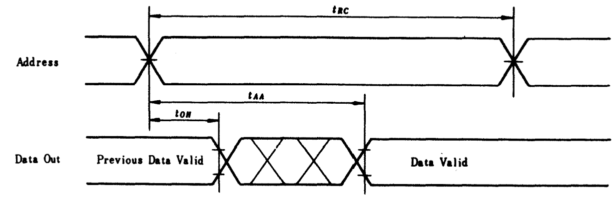
●READ CYCLE

Item	Symbol	HM6167LP		HM6167LP-6		HM6167LP-8		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	70	—	85	—	100	—	ns
Address Access Time	t_{AA}	—	70	—	85	—	100	ns
Chip Select Access Time	t_{ACS}	—	70	—	85	—	100	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	35	—	40	—	45	ns

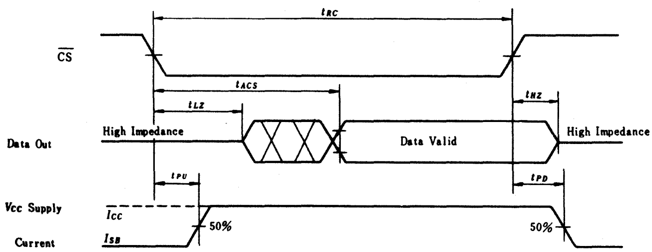
●WRITE CYCLE

Item	Symbol	HM6167LP		HM6167LP-6		HM6167LP-8		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	70	—	85	—	100	—	ns
Chip Selection to End of Write	t_{CW}	55	—	65	—	80	—	ns
Address Valid to End of Write	t_{AW}	55	—	65	—	80	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	40	—	45	—	55	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	30	—	35	—	40	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enable to Output in High Z	t_{WZ}	0	30	0	40	0	40	ns
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns

●TIMING WAVEFORM OF READ CYCLE NO.1 [1),2)]

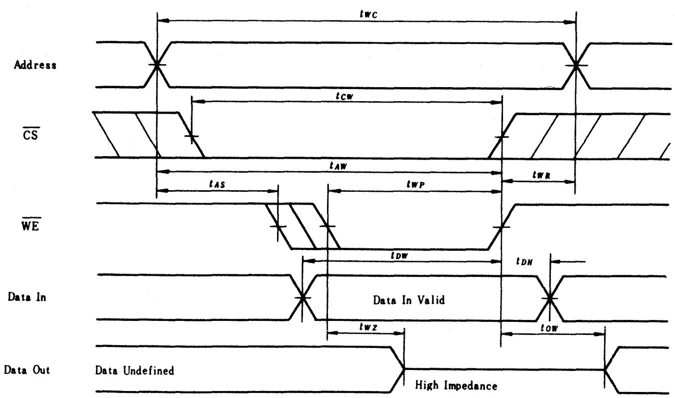


●TIMING WAVEFORM OF READ CYCLE NO.2 [1),3)]



NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ Cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading B.

●TIMING WAVEFORM OF WRITE CYCLE



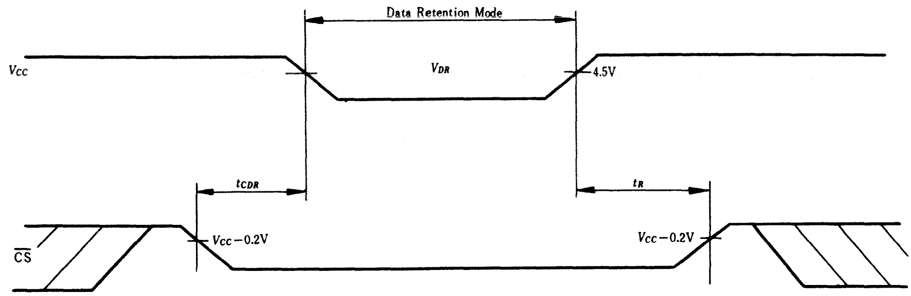
■LOW Vcc DATA RETENTION CHARACTERISTICS (Ta=0°C to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	20*	μA
			—	—	30**	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}△	—	—	ns

△ t_{RC} = Read Cycle Time

* V_{CC}=2.0V
** V_{CC}=3.0V

■LOW Vcc DATA RETENTION WAVEFORM



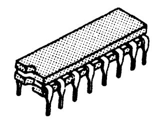
MOS DYNAMIC RAM

HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4

16384-word × 1-bit Dynamic Random Access Memory

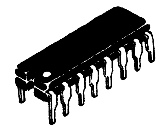
The HM4716A is a 16,384 word by 1 bit MOS random access memory circuit fabricated with HITACHI's double poly N-channel silicon gate process for high performance and high functional density. The HM4716A uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation. Multiplexed address inputs permit the HM4716A to be packaged in a standard 16 pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The HM4716A is designed to facilitate upgrading of the 16-pin 4K RAM. However, the data output latch incorporated in the present 4K design is not appropriate for 16K RAM's. This new generation of memory products (16K RAM's) requires a slightly modified output stage to allow more system flexibility. Instead of the conventional latch, the HM4716A output is controlled by the Column Address Storobe ($\overline{CE}$). Data out of the HM4716A will remain valid from the access time from the Column Address Strobe until $\overline{CE}$ goes into precharge logic 1). However, in early write cycles ($\overline{W}$ active low before $\overline{CE}$ goes low), the data output will remain in the high impedance (open-circuit) state throughout the entire cycle. This type of output operation results in some very significant system implications.

HM4716A-1, HM4716A-2,
HM4716A-3, HM4716A-4



(DG-16A)

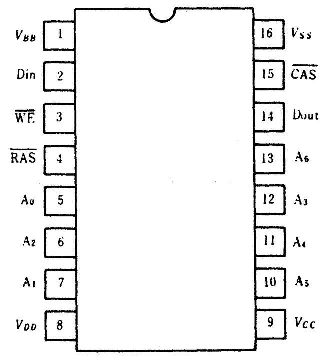
HM4716AP-1, HM4716AP-2,
HM4716AP-3, HM4716AP-4



(DP-16)

1. Common I/O Operation
If all write operation are handled in the "early write" mode, then data in can be connected directly to data-out on a printed circuit board.
2. Data Output Control
Data will remain valid at the output during a read cycle from TCELQV until $\overline{CE}$ returns to precharge.
This allows data to be valid from one cycle up until a new memory cycle begins.
3. Two Methods of Chip Selection
Both $\overline{CE}$ and/or $\overline{RE}$ can be decoded for chip selection.
4. Refresh
Refreshing can be accomplished every 2 ms by either of the two following methods:
(1) normal read or write cycles on 128 addresses, A0 to A6.
(2) $\overline{RE}$ only cycles on 128 addresses, A0 to A6.
A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.
$\overline{RE}$ only refreshes results in a substantial reduction in operating power.
5. Page Mode Operation
The HM4716A is designed for page mode operation.

■ PIN ARRANGEMENT



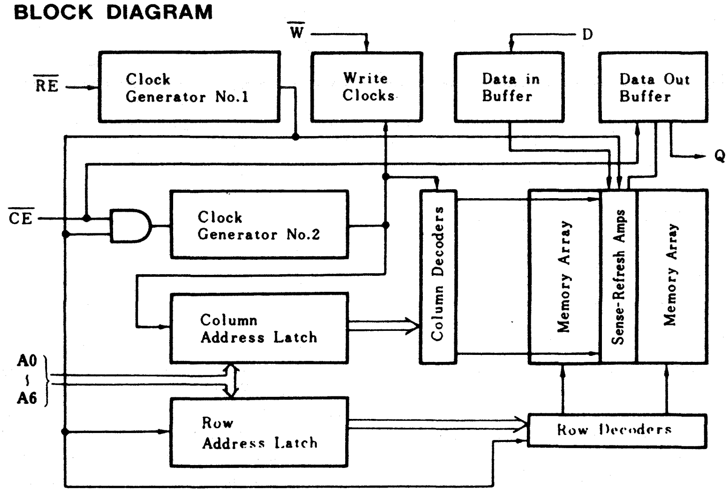
(Top View)

Old	New	Definitions
A_0-A_6	A0-A6	Address Inputs
$\overline{CAS}$	$\overline{CE}$	Column Address Strobe
D_{IN}	D	Data In
D_{OUT}	Q	Data Out
$\overline{RAS}$	$\overline{RE}$	Row Address Strobe
$\overline{WRITE}$	$\overline{W}$	Read/Write Input
V_{BB}	VBB	Power (−5V)
V_{CC}	VCC	Power (+5V)
V_{DD}	VDD	Power (+12V)
V_{SS}	VSS	Ground

■ FEATURES

- All Inputs Including Clocks TTL Compatible
- Input Latches for Address and Data in
- Three-State TTL Compatible Output
- Common I/O Capability
- Only 128 Refresh Cycles Required Every 2ms
- Standard Power Supplies +12V, +5V, −5V (All with 10% tolelance)
- Maximum Access Time
  - HM4716A-1 .... 120ns
  - HM4716A-2 .... 150ns
  - HM4716A-3 .... 200ns
  - HM4716A-4 .... 250ns
- Read or Write Cycle Time
  - HM4716A-1 .... 320ns
  - HM4716A-2 .... 320ns
  - HM4716A-3 .... 375ns
  - HM4716A-4 .... 410ns

■ FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any Pin Relative to VBB .... -0.5V to +20V
Voltage on VDD, VCC Supplies Relative to VSS .... -0.5V to +15V
Voltage on Q Pin Relative to VSS .... -0.5V to +10V
Operating Temperature, TA (Ambient) .... 0°C to +70°C
Storage Temperature (Ambient)* .... -65°C to +150°C
Short-Circuit Output Current 50mA
Power Dissipation 1W

* In case of HM4716AP Series are -55°C to +125°C.

■ RECOMMENDED DC OPERATING CONDITIONS (TA = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	VDD	10.8	12.0	13.2	V	1
	VCC	4.5	5.0	5.5	V	
	VSS	0	0	0	V	
	VBB	−4.5	−5.0	−5.5	V	
Input High (logic 1) Voltage $\overline{RE}$, $\overline{CE}$, $\overline{W}$	VIHC	2.7	—	6.5	V	1
Input High (logic 1) Voltage All inputs except $\overline{RE}$, $\overline{CE}$, $\overline{W}$	VIH	2.4	—	6.5	V	1
Input Low (logic 0) Voltage all inputs	VIL	−1.0	—	0.8	V	1

■ DC ELECTRICAL CHARACTERISTICS

(Ta=0 to +70°C, V_{DD}=12V±10%, V_{CC}=5V±10%, V_{BB}=−5V±10%, V_{SS}=0V)

Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT	I_{DD1}	−	35	mA	2
Average Power Supply Operating Current	I_{CC1}	−	−	mA	3
($\overline{RE}$, $\overline{CE}$ Cycling; TRELREL=375ns)	I_{BB1}	−	300	μA	2
STANDBY CURRENT	I_{DD2}	−	1.5	mA	
Power Supply Standby Current	I_{CC2}	−10	10	μA	5
($\overline{RE}$=$\overline{CE}$=V_{IHC})	I_{BB2}	−	100	μA	
REFRESH CURRENT	I_{DD3}	−	27	mA	2
Average Power Supply Current, Refresh Mode	I_{CC3}	−10	10	μA	5
($\overline{RE}$ Cycling, $\overline{CE}$=V_{IHC}; TRELREL=375ns)	I_{BB3}	−	300	μA	2
PAGE MODE CURRENT	I_{DD4}	−	27	mA	
Average Power Supply Current, Page-mode Operation	I_{CC4}	−	−	mA	3
($\overline{RE}$=V_{IL}, $\overline{CE}$ Cycling; TCELCEL=225ns)	I_{BB4}	−	300	μA	
INPUT LEAKAGE Input Leakage Current, any Input (V_{BB}=−5V, V_{IN}=0 to +7V, all other pins not under test=0V)	I_{IL}	−10	10	μA	
OUTPUT LEAKAGE Output Leakage Current (Q is Disabled, V_{OUT}=0 to +5.5V)	I_{OL}	−10	10	μA	5
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{OUT}=−5mA)	V_{OH}	2.4	V_{CC}	V	4
Output Low (Logic 0) Voltage (I_{OUT}=4.2mA)	V_{OL}	0	0.4	V	

NOTES

1. All voltages referenced to VSS, VBB must be applied before and removed after other supply voltage.
2. Current depend on cycle rate: maximum current is measured at the fastest cycle rate.
3. ICC depends upon output loading. The VCC supply is connected to the output buffer only.
4. Output voltage will swing from VSS to VCC when activated with no current loading. For purposes of maintaining data in standby mode, VCC may be reduced to VSS without affecting refresh operations or data retention. However, the VOH (min) specification is not guaranteed in this mode.
5. ICC2, ICC3 and IOL consists of leakage current only.
6. AC measurements assume TT = 5ns.
7. VIHC (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIHC or VIH and VILS.
8. Assumes that TRELCEL = TRELCEL (max.) If TRELCEL is greater than the maximum recommended value shown in this table, TRELQV exceeds the value shown.
9. Assumes that TRELCEL = TRELCEL (max).
10. Measured with a load circuit equivalent to 2TTL loads and 100pF (in case of HM4716A-2:1 TTL and 50pF). And VSS + 0.8V, VSS + 2.0V are the reference level for measuring timing of Q.
11. TCEHQZ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation with the TRELCEL (max) limit insures that TRELQC (max) can be met TRELCEL (max) is specified as a reference point only; if TRELCEL is greater than the specified TRELCEL (max) limit, then access time is controlled exclusively by TCELQV.
13. These parameters are reference to $\overline{CE}$ leading edge in early write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
14. TWLCEL, TCELWL and TRELWL are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if TWLCEL = TWLCEL (min), the cycle is an early write and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if TCELWL = TCELWL (min) and TRELWL will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
15. Capacitance measured with Boonton Meter or effective capacitance measuring methods.)
16. $\overline{CE}$ = VIHC to disable Q.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70℃, V_{DD}=12V±10%, V_{CC}=5V±10%, V_{SS}=0V, V_{BB}=−5V±10%)

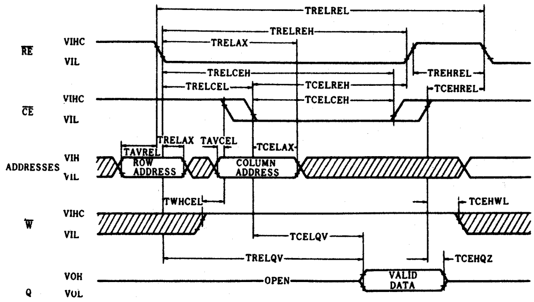
Parameter	Symbol		HM4716A-1		HM4716A-2		HM4716A-3		HM4716A-4		Unit	Notes
	Old	New	min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	TRELREL	320	—	320	—	375	—	410	—	ns	
Read-Write Cycle Time	t_{RWC}	TRELREL	320	—	320	—	375	—	515	—	ns	8
Page Mode Cycle Time	t_{PC}	TCELCEL	160	—	170	—	225	—	275	—	ns	
Access Time From $\overline{RE}$	t_{RAC}	TRELQV	—	120	—	150	—	200	—	250	ns	8, 10
Access Time From $\overline{CE}$	t_{CAC}	TCELQV	—	80	—	100	—	135	—	165	ns	9, 10
Output Buffer Turn-off Delay	t_{OFF}	TCEHQZ	0	35	0	50	0	60	0	70	ns	11
Transition Time (Rise and Fall)	t_T	TT	3	35	3	35	3	50	3	50	ns	7
$\overline{RE}$ Precharge Time	t_{RP}	TREHREL	100	—	100	—	120	—	150	—	ns	
$\overline{RE}$ Pulse Width	t_{RAS}	TRELREH	120	10000	150	10000	200	10000	250	10000	ns	
$\overline{RE}$ Hold Time	t_{RSH}	TCELREH	80	—	100	—	135	—	165	—	ns	
$\overline{CE}$ Pulse Width	t_{CAS}	TCELCEH	80	10000	100	10000	135	10000	165	10000	ns	
$\overline{CE}$ Hold Time	t_{CSH}	TRELCEH	120	—	150	—	200	—	250	—	ns	
$\overline{RE}$ to $\overline{CE}$ Delay Time	t_{RCD}	TRELCEL	15	40	25	50	30	65	40	85	ns	12
$\overline{CE}$ to $\overline{RE}$ Precharge Time	t_{CRP}	TCEHREL	0	—	−20	—	−20	—	−20	—	ns	
Row Address Set-up Time	t_{ASR}	TAVREL	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	TRELAX	15	—	20	—	25	—	35	—	ns	
Column Address Set-up Time	t_{ASC}	TAVCEL	−5	—	−5	—	−5	—	−5	—	ns	
Column Address Hold Time	t_{CAH}	TCELAX	40	—	45	—	55	—	75	—	ns	
Column Address Hold Time Reference to $\overline{RE}$	t_{AR}	TRELAX	80	—	95	—	120	—	160	—	ns	
Read Command Set-up Time	t_{RCS}	TWHCEL	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	TCEHWL	0	—	20	—	20	—	20	—	ns	
Write Command Hold Time	t_{WCH}	TCELWH	40	—	45	—	55	—	75	—	ns	
Write Command Hold Time Reference $\overline{RE}$	t_{WCR}	TRELWH	80	—	95	—	120	—	160	—	ns	
Write Command Pulse Width	t_{WP}	TWLWH	40	—	45	—	55	—	75	—	ns	
Write Command to $\overline{RE}$ Lead Time	t_{RWL}	TWLREH	50	—	60	—	80	—	100	—	ns	
Write Command to $\overline{CE}$ Lead Time	t_{CWL}	TWLCEH	50	—	60	—	80	—	100	—	ns	
Data-in Set-up Time	t_{DS}	TDVCEL	0	—	0	—	0	—	0	—	ns	13
Data-in Hold Time	t_{DH}	TCELDX	40	—	45	—	55	—	75	—	ns	13
Data-in Hold Time Referenced $\overline{RE}$	t_{DHR}	TRELDX	80	—	95	—	120	—	160	—	ns	
$\overline{CE}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	TCEHCEL	60	—	60	—	80	—	100	—	ns	
Refresh Period	t_{REF}	TRVRV	—	2	—	2	—	2	—	2	ms	
$\overline{W}$ Command Set-up Time	t_{WCS}	TWLCEL	0	—	−20	—	−20	—	−20	—	ns	14
$\overline{CE}$ to $\overline{RE}$ Delay	t_{CWD}	TCELWL	60	—	70	—	95	—	125	—	ns	14
$\overline{RE}$ to $\overline{W}$ Delay	t_{RWD}	TRELWL	100	—	120	—	160	—	200	—	ns	14
$\overline{RE}$ Precharge to $\overline{CE}$ Hold Time	t_{RPC}	TREHCEL	0	—	0	—	0	—	0	—	ns	

■ AC ELECTRICAL CHARACTERISTICS

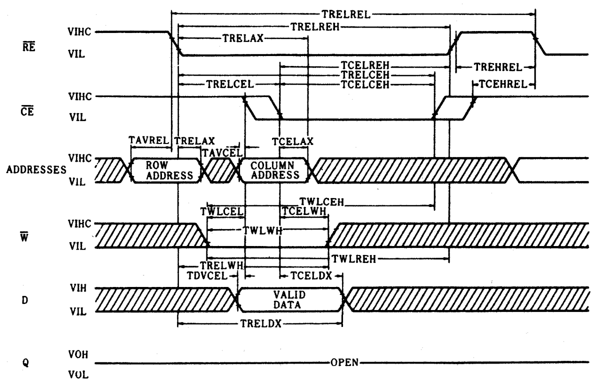
Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (A_0-A_6, D)	C_{I1}	—	5	pF	15
Input Capacitance $\overline{RE}$, $\overline{CE}$, $\overline{W}$	C_{I2}	—	10	pF	15
Output Capacitance (Q)	C_Q	—	7	pF	15, 16

■ TIMING WAVEFORMS

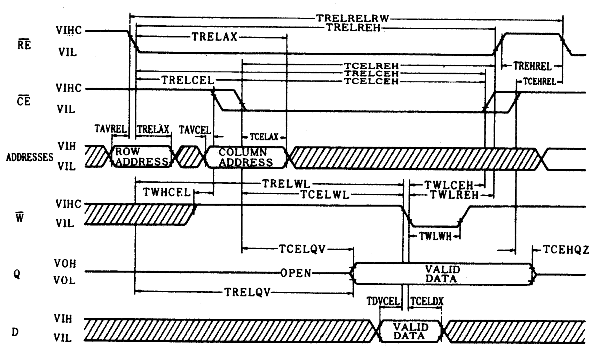
● READ CYCLE



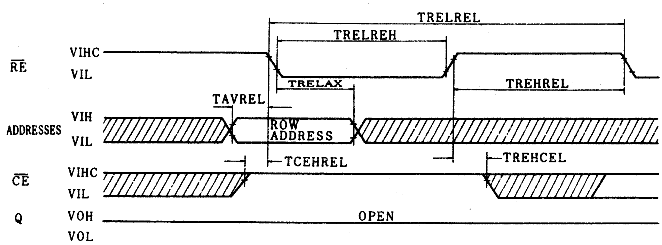
● WRITE CYCLE (EARLY WRITE)



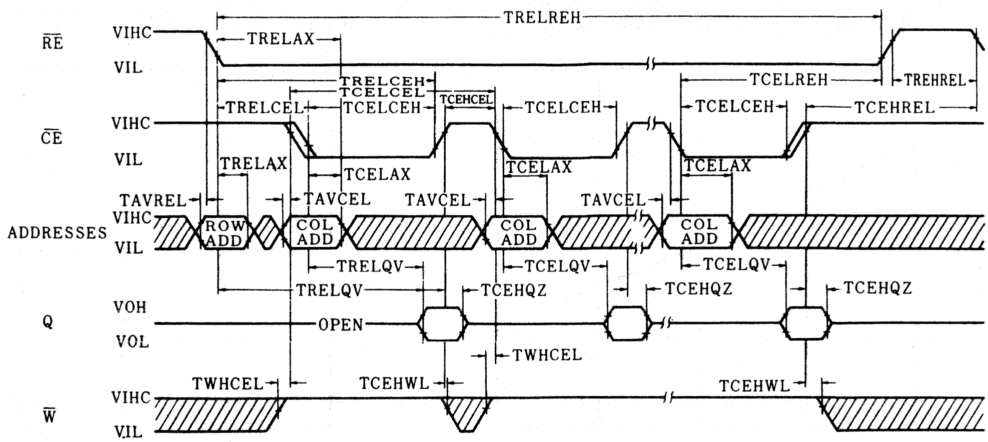
● READ-WRITE/READ-MODIFY-WRITE CYCLE



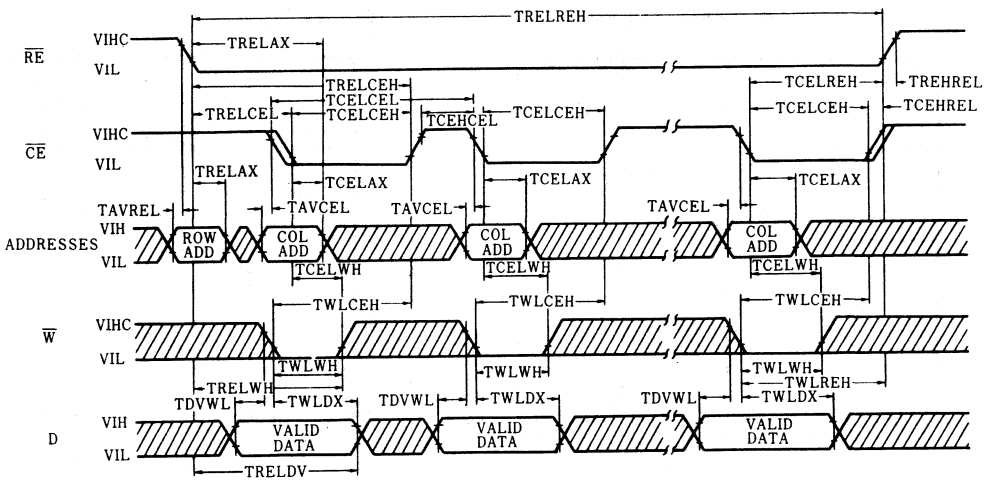
● "$\overline{RE}$ ONLY" REFRESH CYCLE



●PAGE MODE READ CYCLE

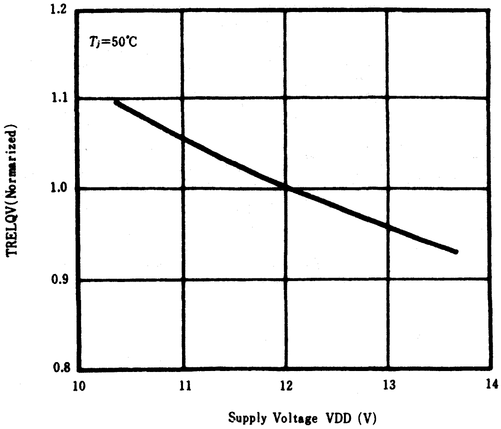


●PAGE MODE WRITE CYCLE

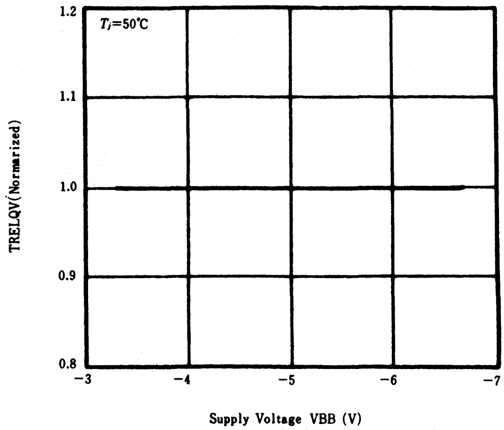


■ TYPICAL CHARACTERISTICS

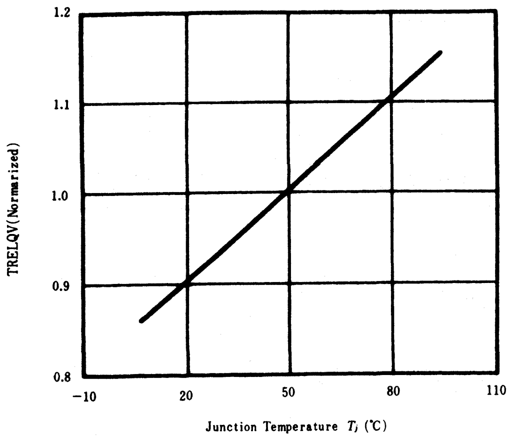
ACCESS TIME (NORMARIZED) vs. V_{DD}



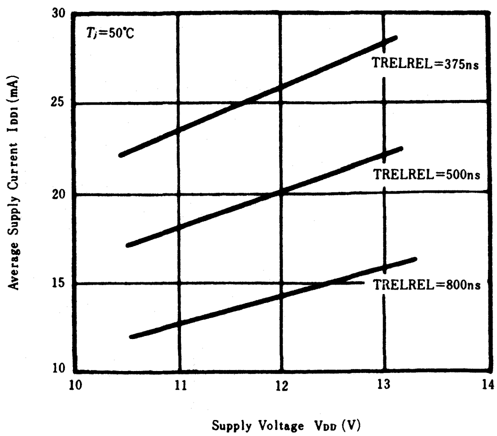
ACCESS TIME (NORMARIZED) vs. V_{BB}



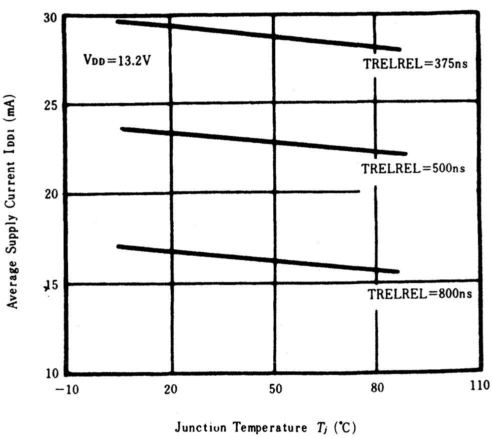
ACCESS TIME (NORMARIZED) vs. T_j



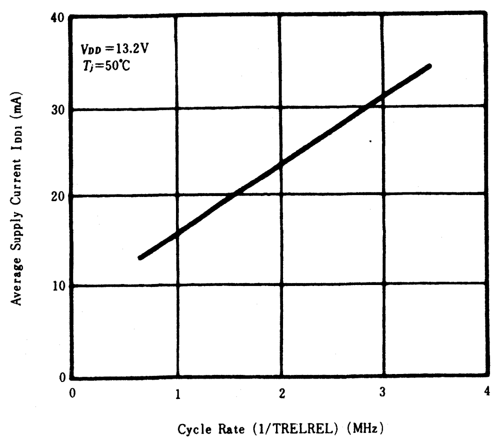
IDDI vs. V_{DD}



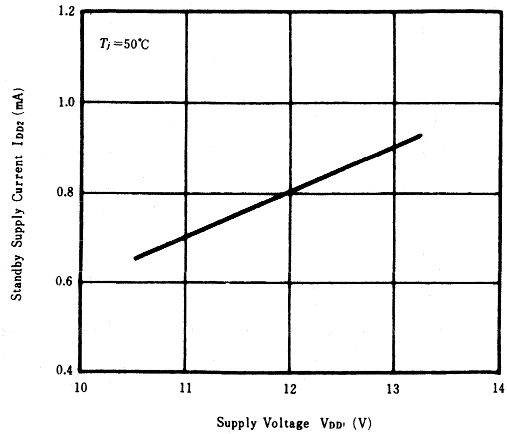
IDDI vs. T_j



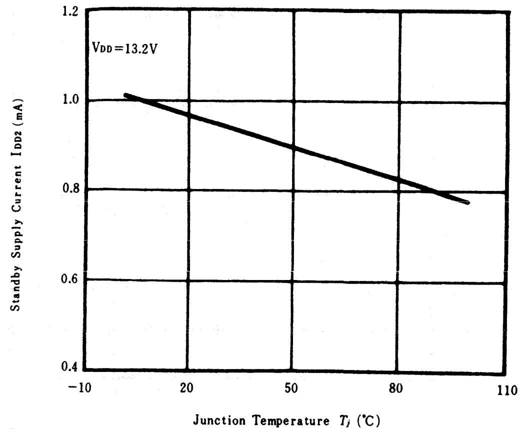
IDDI vs. CYCLE RATE



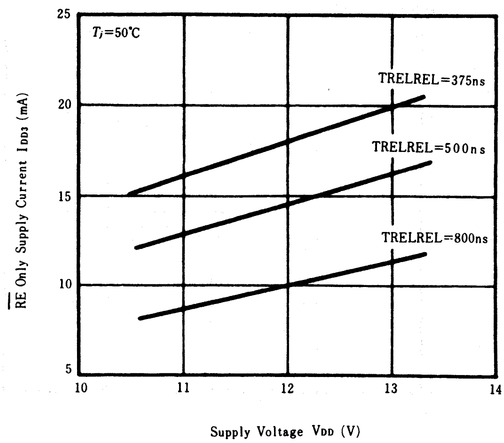
IDD2 (STANDBY) vs. V_{DD}



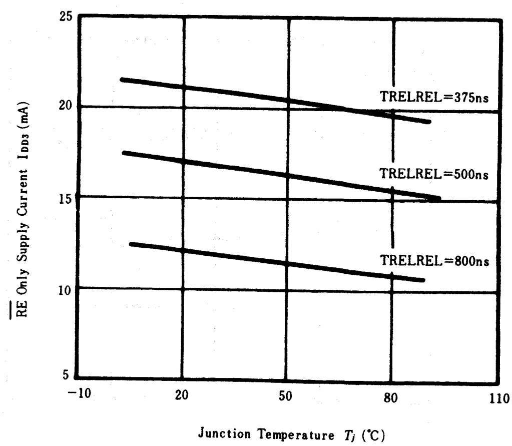
IDD2 (STANDBY) vs. T_j



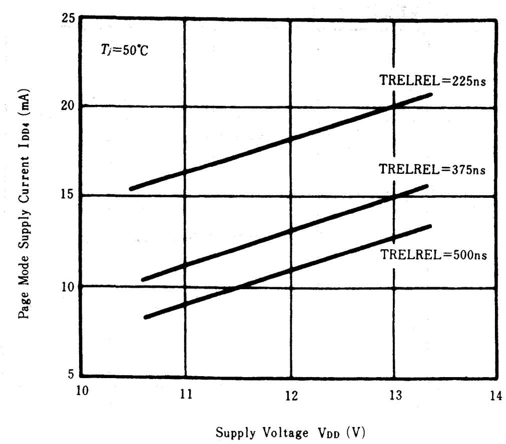
IDD3 ($\overline{RE}$ ONLY CYCLE) vs. V_{DD}



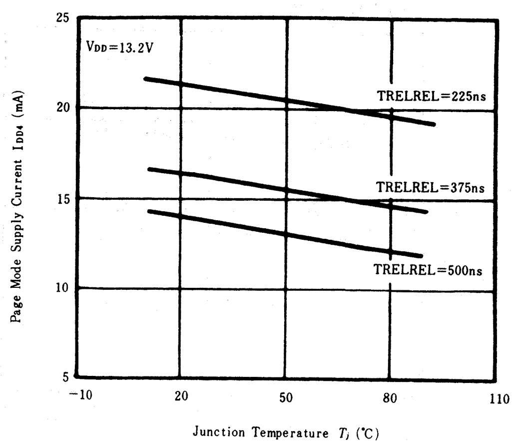
IDD3 ($\overline{RE}$ ONLY CYCLE) vs. T_j



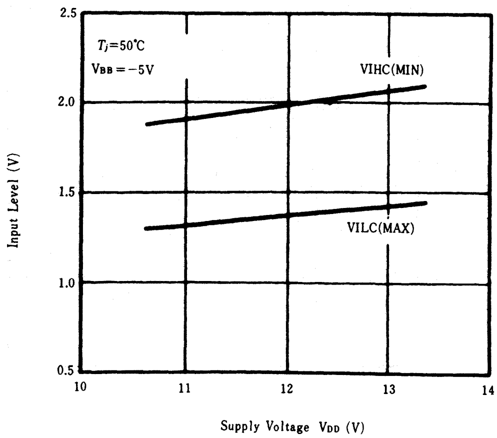
IDD4 (PAGE-MODE CYCLE) vs. V_{DD}



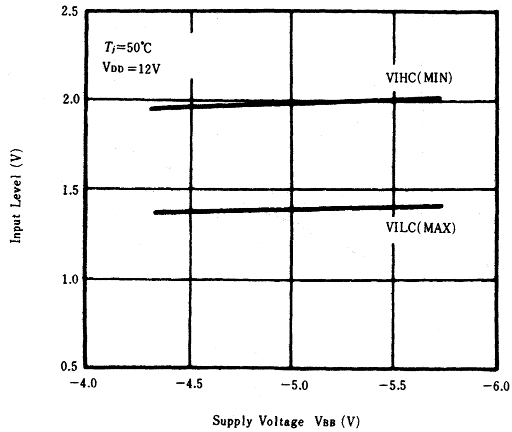
IDD4 (PAGE-MODE CYCLE) vs. T_j



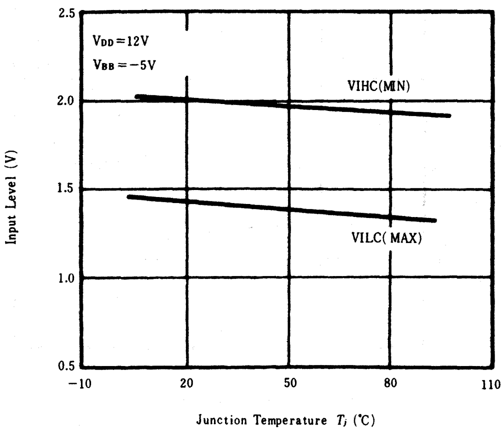
CLOCK INPUT LEVELS vs. V_{DD}



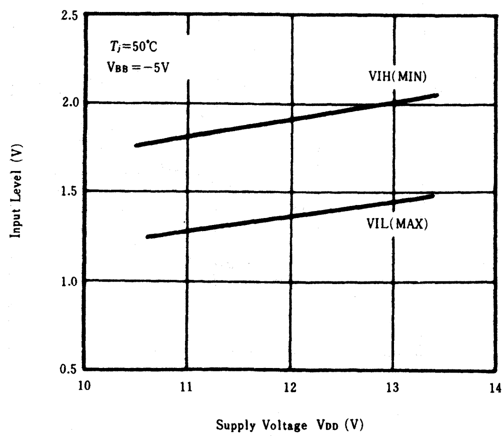
CLOCK INPUT LEVELS vs. V_{BB}



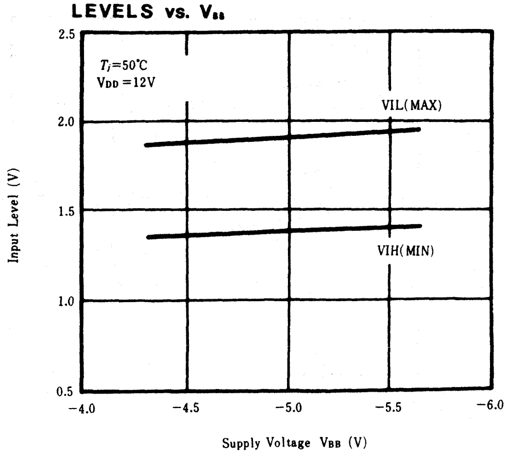
CLOCK INPUT LEVELS vs. T_j



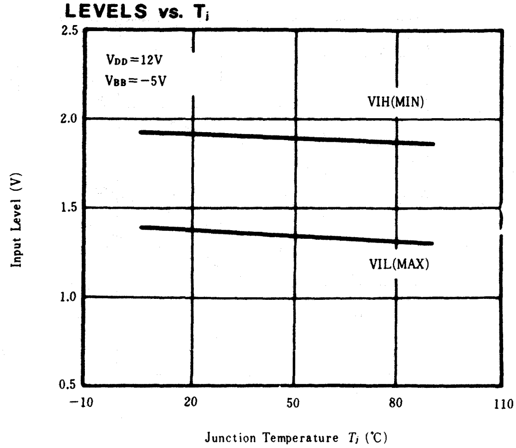
ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



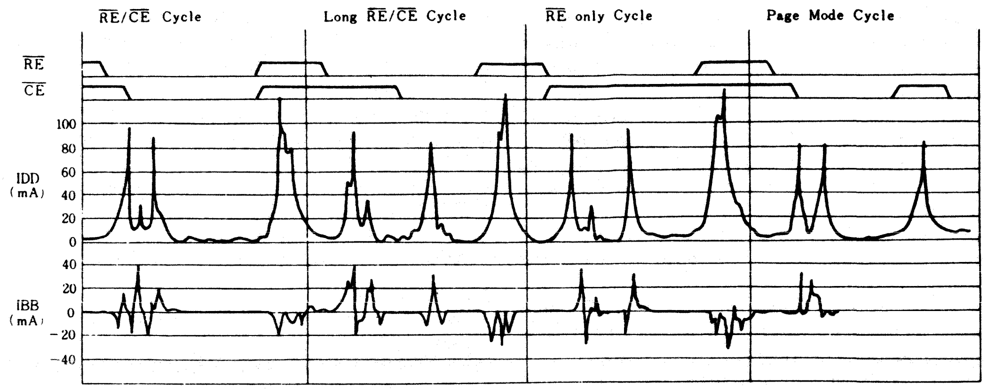
ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



ADDRESS AND DATA INPUT LEVELS vs. T_j



■ CURRENT WAVEFORMS



NOTE : VDD = 13.2V, VBB = −4.5V, Ta = 25°C

50ns

APPLICATION INFORMATION

• READ CYCLE;

A read cycle begins with addresses stable and a negative going transistion of $\overline{RE}$. The time delay between the stable address and the start of $\overline{RE}$-on is controlled by parameter TAVREL.

Following the time when $\overline{RE}$ reaches its low level, the row address must be held stable long enough to be captured.

This controlling parameter is TRELAX. Following this interval, the address can be changed from row address to column address.

When the column address is stable, $\overline{CE}$ can be turned on.

The leading edge of $\overline{CE}$ is controlled by parameter TRELCEL.

The basic limit on the $\overline{CE}$ leading edge is that $\overline{CE}$ cannot start until the column address is stable, and this is controlled by parameter TAVCEL.

The column address must be held stable long enough to be captured.

The controlling parameter is TCELAX. Note that TRELCEL(max) is not an operating limit of the HM4716A though its specification is listed on the data sheets. If $\overline{CE}$ becomes on later than TRELCEL(max), the access time from $\overline{RE}$ will be increased by the time which TRELCEL exceeds TRELCEL(max).

Following the time when $\overline{CE}$ reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is TCELQV-access time from $\overline{CE}$. The access time from $\overline{RE}$-TRELQV is the time from $\overline{RE}$-on to valid Q. The minimum value of TRELQV is derived as the sum of TRELCEL(max) and TCELQV. The selected output data is held valid internally until $\overline{CE}$ becomes high, and then Q pin becomes high impedance. This parameter is TECHQZ.

• WRITE CYCLE;

A write cycle is performed by bringing $\overline{W}$ low before or during $\overline{CE}$-on.

Two different write cycles can be defined as;

Write cycle — Write data are available at the beginning of the $\overline{CE}$-on so that the write operation starts at the beginning. In this mode, D and $\overline{W}$ signal times are not in any critical path for determining cycle time.

Following the time when $\overline{W}$ reaches its low level. $\overline{W}$ must be held stable long enough to be captured. This $\overline{W}$-on pulse duration is called TWLWH.

The time required to capture write data in a latch is called TWLDX.

This cycle is called an "early write"

Read Write cycle — This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated. $\overline{W}$ and D are delayed until after Q. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, D and $\overline{W}$ become critical path signals for determining cycle time.

• CLOCK-OFF TIMING;

$\overline{RE}$ and $\overline{CE}$ must stay on for Q stabilized to valid data. In the case of $\overline{CE}$, this is controlled by parameter TCELCEH (min). In the case of $\overline{RE}$, this controlled by parameter TCELREH(min).

Following the end of $\overline{RE}$, $\overline{CE}$ must stay off long enough to precharge internal circuits. The only parameter of concern is TREHREL.

Normally $\overline{CE}$ is not required to be off for a minimum time of TCEHREL.

However, in a page mode memory operation, there is a TCEHCEL(min) specification to control the $\overline{CE}$-off time.

• DATA OUTPUT;

Q is three-state TTL compatible with a fan-out of two standard TTL loads.

When $\overline{CE}$ is high, Q is in a high impedance state. When $\overline{CE}$ is low, valid data appears after TCELQV at a read cycle and Q is not valid at an early-write cycle.

• REFRESH;

Refresh of the HM4716A is accomplished by performing A memory cycle at each of the 128 row addresses within each two millisecond time interval.

Any cycle in which $\overline{RE}$ signal occurs refreshes the entire selected row.

$\overline{RE}$-only refresh results in substantial reduction in operating power.

This reduction in power is reflected in the IDD3 specification.

• PAGE MODE;

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining $\overline{RE}$ at a logic low throughout all successive $\overline{CE}$ memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be decreased and the operating power is reduced. These are reflected in the TCELQV, TCEHCEL, IDD4 specifications.

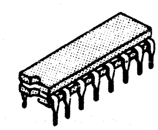
HM4816A-3, HM4816A-3E, HM4816A-4, HM4816A-7, HM4816AP-3, HM4816AP-3E, HM4816AP-4, HM4816AP-7

16384-word by 1-bit Dynamic Random Access Memory

The HM4816A is a new generation MOS dynamic RAM circuit organized as 16,384 words by 1 bit. As a state-of-the art MOS memory device, the HM4816A (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power.

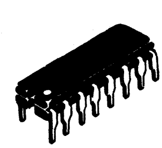
The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the HM4816A a truly superior RAM product. Multiplexed address inputs permits the HM4816A to be packaged in standard 16-pin DIP. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

HM4816A-3, HM4816A-3E,
HM4816A-4, HM4816A-7



(DG-16B)

HM4816AP-3, HM4816AP-3E,
HM4816AP-4, HM4816AP-7



(DP-16)

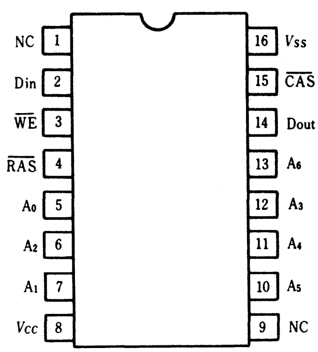
■ FEATURES

- Single 5V supply
  Low power standby and operation
  (Standby: 11mW max., operation: 150mW max.)
- Fast access time & cycle time

	HM4816A-3 HM4816AP-3	HM4816A-3E HM4816AP-3E	HM4816A-4 HM4816AP-4	HM4816A-7 HM4816AP-7
Maximum Access Time (ns)	100	105	120	150
Read, Write Cycle (ns)	235	200	270	320
Read-Modify-Write Cycle (ns)	285	235	320	410

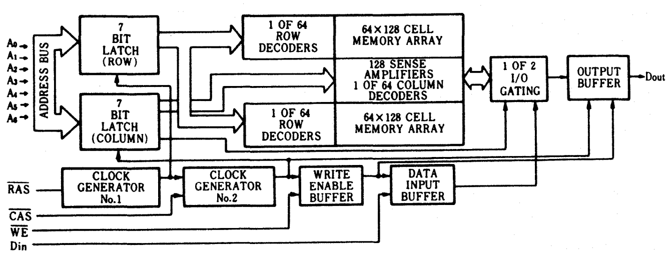
- Directly TTL compatible: All inputs & outputs
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary.
- Common I/O capability using "easy write" operation.
- Read modify write, $\overline{RAS}$ only refresh and page mode capability
- Only 128 refresh cycle required every 2ms
- Compatible with Intel 2118-3/-4/-7

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	HM4816A or AP	Unit
Voltage on any pin relative to GND		V_T	$-1.0 \sim +7.0$	V
Power supply voltage relative to GND		V_{CC}	$-0.5 \sim +7.0$	V
Short-circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	1.0	W
Operating Temperature		T_{opr}	$0 \sim +70$	℃
Storage Temperature	Cerdip	T_{stg}	$-65 \sim +150$	℃
	Plastic		$-55 \sim +125$	℃

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1, 2
Input high (logic 1) voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IHC}	2.4	—	7.0	V	1
Input high (logic 1) voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IH}	2.4	—	7.0	V	1
Input low (logic 0) voltage all inputs	V_{IL}	-2.0	—	0.8	V	1

Notes : 1. All voltage referenced to V_{SS}.
2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading.

■ DC AND OPERATING CHARACTERISTICS (1)

($Ta=0$℃ to 70℃, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted.)

Parameter	Symbol	Test Conditions		min	typ (2)	max	Unit	Notes
Input Load Current (any input)	$\lvert I_{LI}\rvert$	$V_{IN}=V_{SS}$ to V_{CC}		—	0.1	10	μA	
Output Leakage Current for High Impedance State	$\lvert I_{LO}\rvert$	Chip Deselected; $\overline{CAS}$ at V_{IH}, $V_{OUT}=0$ to 5.5V		—	0.1	10	μA	
V_{CC} Supply Current. Standby	I_{CC1}	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	HM4816AP-3, 4, 7 HM4816A-3, 4, 7	—	1.2	2	mA	
			HM4816A, AP-3E	—	1.2	3	mA	
V_{CC} Supply Current. Operating	I_{CC2}	HM4816A, AP-3 $t_{RC}=t_{RCMIN}$		—	23	27	mA	3
		HM4816A, AP-3E $t_{RC}=t_{RCMIN}$		—	27	35	mA	3
		HM4816A, AP-4 $t_{RC}=t_{RCMIN}$		—	21	25	mA	3
		HM4816A, AP-7 $t_{RC}=t_{RCMIN}$		—	19	23	mA	3
V_{CC} Supply Current; $\overline{RAS}$-Only Cycle	I_{CC3}	HM4816A, AP-3 $t_{RC}=t_{RCMIN}$		—	16	18	mA	3
		HM4816A, AP-3E $t_{RC}=t_{RCMIN}$		—	20	25	mA	3
		HM4816A, AP-4 $t_{RC}=t_{RCMIN}$		—	14	16	mA	3
		HM4816A, AP-7 $t_{RC}=t_{RCMIN}$		—	12	14	mA	3
V_{CC} Supply Current. Standby. Output Enabled	I_{CC5}	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}		—	3	6	mA	3
Output Low Voltage	V_{OL}	$I_{OL}=4.2mA$		—	—	0.4	V	
Output High Voltage	V_{OH}	$I_{OH}=-5mA$		2.4	—	—	V	

Notes : 1. All voltages referenced to V_{SS}.
2. Typical values are for $Ta=25$℃ and nominal supply voltages.
3. I_{CC} is dependent on output loading when the devices output is selected. Specified I_{CC} MAX is measured with the output open.

■ CAPACITANCE

($Ta=25$℃, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted.)

Parameter	Symbol	typ	max	Unit
Address. Data In	C_{I1}	3	5	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, Data Out	C_{I2}	4	7	pF

Notes : Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$C=\frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.

■ AC CHARACTERISTICS [1,2,3] (Ta=0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

● READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Parameter	Symbol	HM4816A-3 HM4816AP-3		HM4816A-3E HM4816AP-3E		HM4816A-4 HM4816AP-4		HM4816A-7 HM4816AP-7		Unit	Notes
		min	max	min	max	min	max	min	max		
Access Time From $\overline{RAS}$	t_{RAC}	—	100	—	105	—	120	—	150	ns	4, 5
Access Time From $\overline{CAS}$	t_{CAC}	—	55	—	60	—	65	—	80	ns	4, 5, 6
Time Between Refresh	t_{REF}	—	2	—	2	—	2	—	2	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	110	—	70	—	120	—	135	—	ns	
$\overline{CAS}$ Precharge Time (non-page cycles)	t_{CPN}	50	—	50	—	55	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0	—	0	—	0	—	0	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	45	25	45	25	55	25	70	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	70	—	60	—	85	—	105	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	105	—	120	—	165	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	15	—	15	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	25	—	20	—	20	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	—	70	—	75	—	90	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	8
Output Buffer Turn Off Delay	t_{OFF}	0	45	0	50	0	50	0	60	ns	

● READ AND REFRESH CYCLES

Parameter	Symbol	min	max	min	max	min	max	min	max	Unit	Notes
Random Read Cycle Time	t_{RC}	235	—	200	—	270	—	320	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	115	10000	105	10000	140	10000	175	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	55	10000	60	10000	65	10000	95	10000	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	10	—	10	—	10	—	10	—	ns	

● WRITE CYCLE

Parameter	Symbol	min	max	min	max	min	max	min	max	Unit	Notes
Random Write Cycle Time	t_{RC}	235	—	200	—	270	—	320	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	115	10000	105	10000	140	10000	175	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	55	10000	60	10000	65	10000	95	10000	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	30	—	30	—	45	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	70	—	75	—	85	—	115	—	ns	
Write Command Pulse Width	t_{WP}	25	—	30	—	30	—	50	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	60	—	45	—	65	—	110	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	—	45	—	50	—	100	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	0	—	ns	
Data-in Hold Time	t_{DH}	25	—	30	—	30	—	45	—	ns	
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	70	—	75	—	85	—	115	—	ns	

● READ-MODIFY-WRITE CYCLE

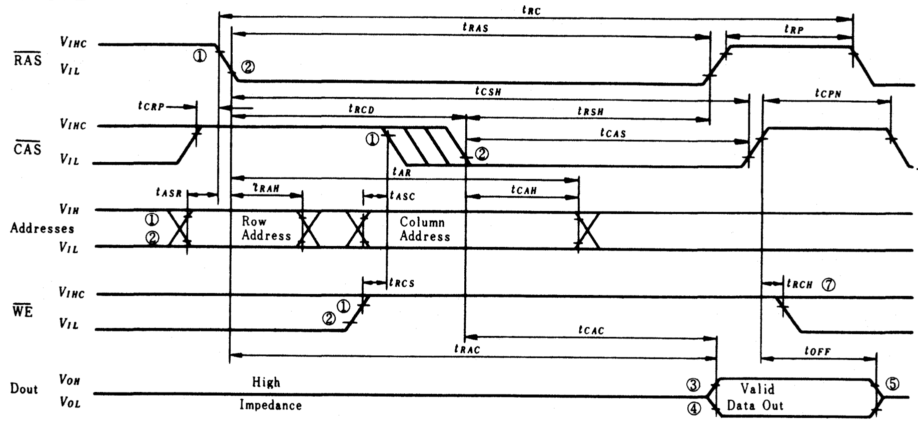
Parameter	Symbol	min	max	min	max	min	max	min	max	Unit	Notes
Read-Modify-Write Cycle Time	t_{RWC}	285	—	235	—	320	—	410	—	ns	
RMW Cycle $\overline{RAS}$ Pulse Width	t_{RRW}	165	10000	155	10000	190	10000	265	10000	ns	
RMW Cycle $\overline{CAS}$ Pulse Width	t_{CRW}	105	10000	110	10000	120	10000	185	10000	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	100	—	105	—	120	—	150	—	ns	9
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	55	—	60	—	65	—	80	—	ns	9

Notes:

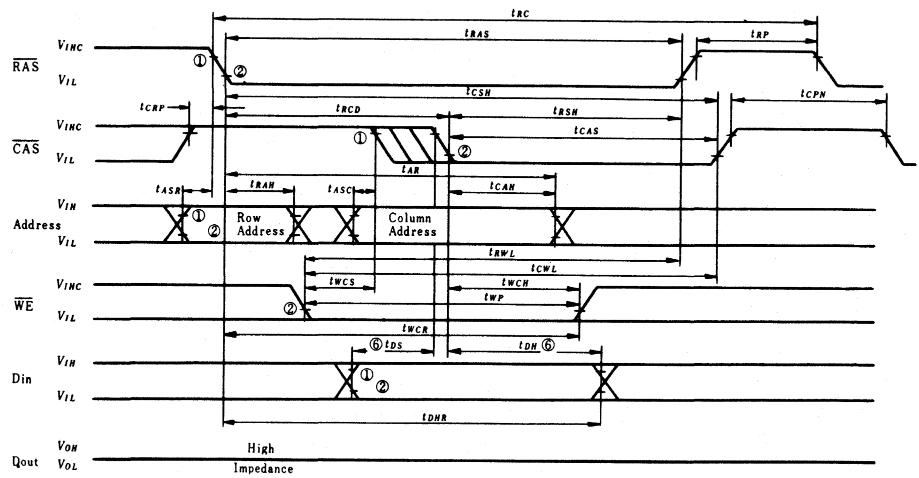
1. All voltages referenced to V_{SS}
2. Eight cycles are required after power-up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purposes.
3. AC Characteristics assume t_T=5ns
4. Assume that $t_{RCD} \leqq t_{RCD}$ (max.) If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.)
5. Load = 2 TTL Loads and 100pF
6. Assumes $t_{RCD} \geqq t_{RCD}$ (max.)
7. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}. If t_{RCD} is greater than t_{RCD} (max.) access time is t_{RCD} + t_{CAC}.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.)
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address if neither of the above conditions is satisfied, the condition on the data out is indeterminate.

■ WAVEFORMS

● READ CYCLE



● WRITE CYCLE



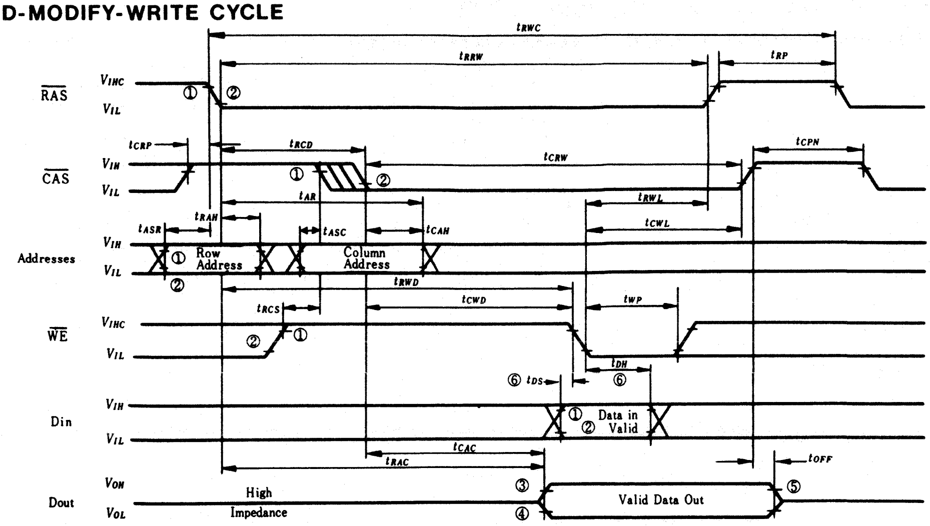
Notes:

1.2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.

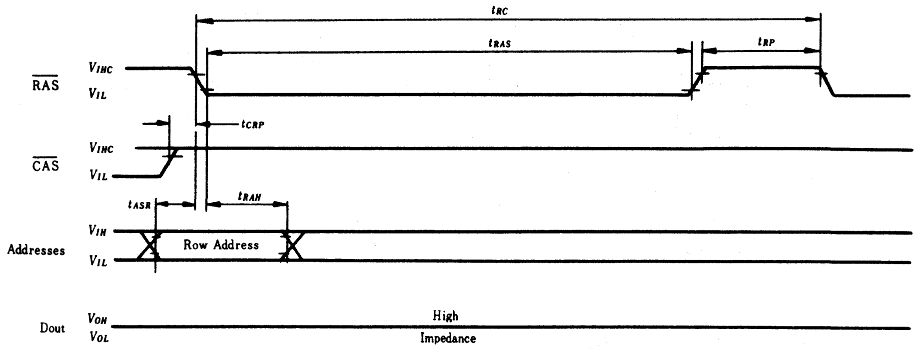
3.4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.

5. t_{OFF} is measured to $I_{OUT} < |I_{LO}|$.
6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{RCH} is referenced to the trailing edge of $\overline{CAS}$ or $\overline{RAS}$, whichever occurs first.
8. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for system where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

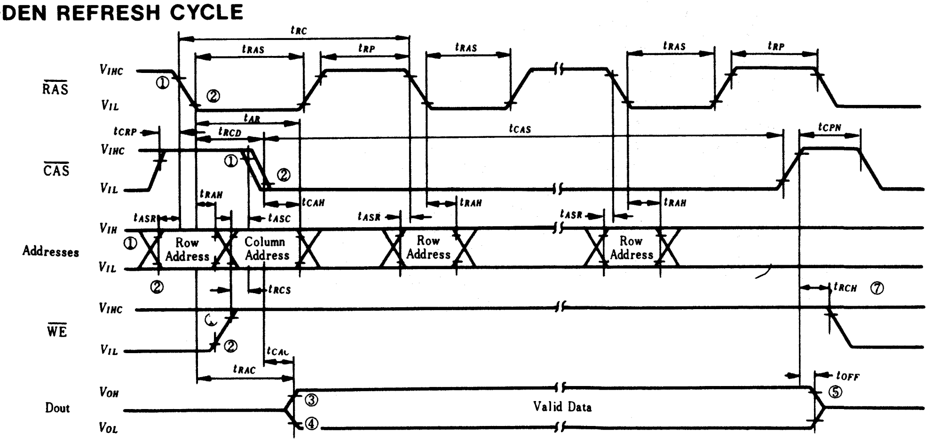
● READ-MODIFY-WRITE CYCLE



● $\overline{\text{RAS}}$-ONLY REFRESH CYCLE



● HIDDEN REFRESH CYCLE



Notes:

1.2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ and reference levels for measuring timing of input signals.

3.4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.

5. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

6. t_{DS} and t_{DH} are referenced to $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs last.

7. t_{RCH} is referenced to the trailing edge of $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$, whichever occurs first.

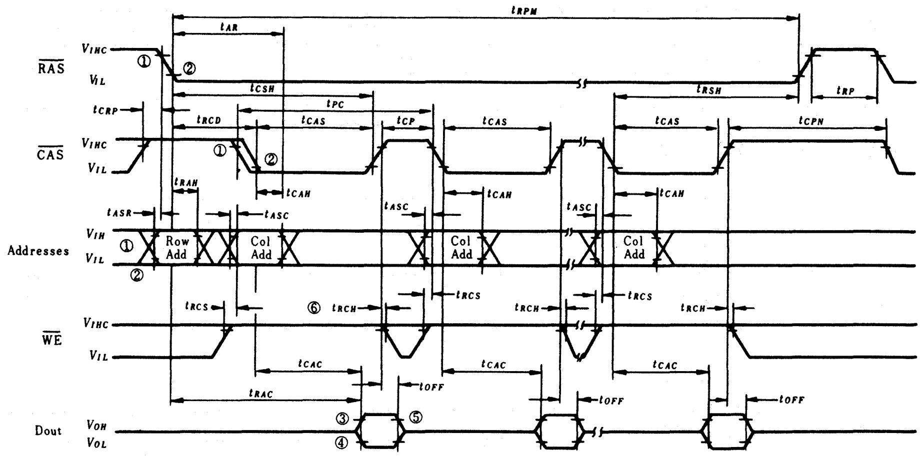
8. t_{CRP} requirement is only applicable for $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles preceeded by a $\overline{\text{CAS}}$-only cycle (i.e., for systems where $\overline{\text{CAS}}$ has not been decoded with $\overline{\text{RAS}}$).

■ DC AND AC CHARACTERISTICS, PAGE MODE [7.8.]

(Ta=0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

Parameter	Symbol	HM4816A-3 HM4816AP-3		HM4816A-3E HM4816AP-3E		HM4816A-4 HM4816AP-4		HM4816A-7 HM4816AP-7		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Page Mode Read or Write Cycle	t_{PC}	125	—	130	—	145	—	190	—	ns
Page Mode Read Modify Write Cycle	t_{PCM}	175	—	180	—	200	—	280	—	ns
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	60	—	60	—	70	—	85	—	ns
$\overline{RAS}$ Pulse Width, Page Mode	t_{RPM}	115	10000	105	10000	140	10000	175	10000	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	55	10000	60	10000	65	10000	95	10000	ns
V_{DD} Supply Current Page Mode. Minimum t_{PC}. Minimum t_{CAS}	I_{DD4}	—	23	—	23	—	21	—	18	mA

● PAGE MODE READ CYCLE



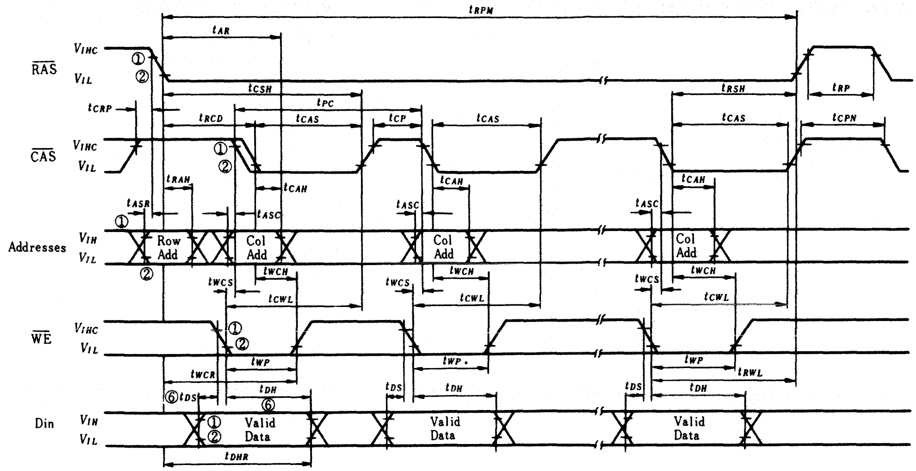
Notes:

1.2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.

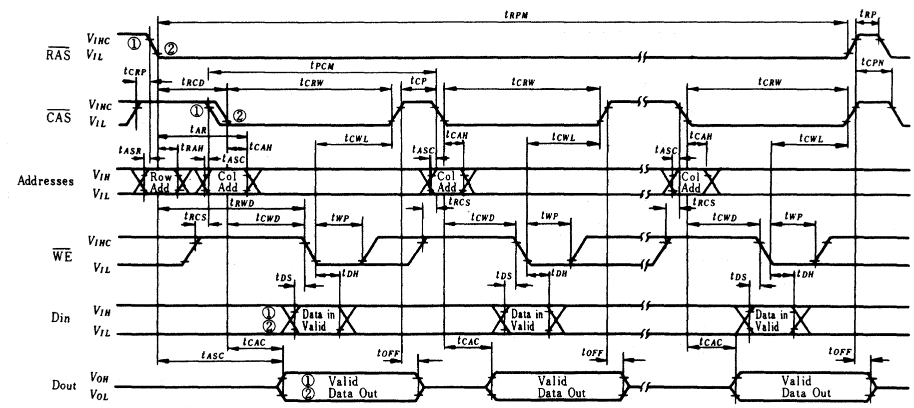
3.4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.

5. t_{OFF} is measured to $I_{OUT} \leqq |I_{LO}|$.
6. t_{RCH} is referenced to the trailing edge of $\overline{CAS}$ or $\overline{RAS}$, whichever occurs first.
7. All voltages referenced to V_{SS}.
8. AC Characteristic assume t_T=5ns.
9. See the typical characteristics section for values of this parameter under alternate conditions.
10. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
11. All previous specified A.C. and D.C. characteristics are applicable to their respective page mode device.

●PAGE MODE WRITE CYCLE



●PAGE MODE READ-MODIFY-WRITE CYCLE



1.2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.

3.4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.

5. t_{OFF} is measured to $I_{OUT} \leqq |I_{LO}|$.

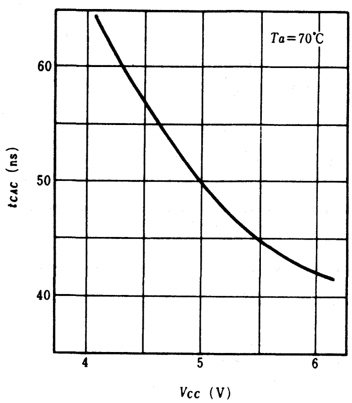
6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

7. t_{RCH} is referenced to the trailing edge of $\overline{CAS}$ or $\overline{RAS}$, whichever occurs first.

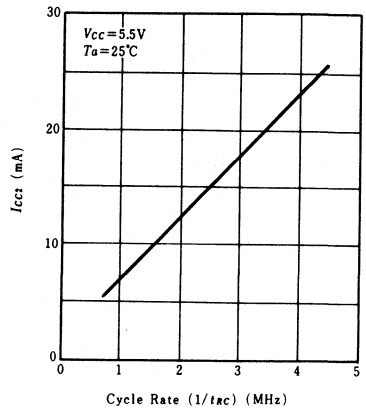
8. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$, cycles preceeded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

● Typical Characteristics of HM4816A

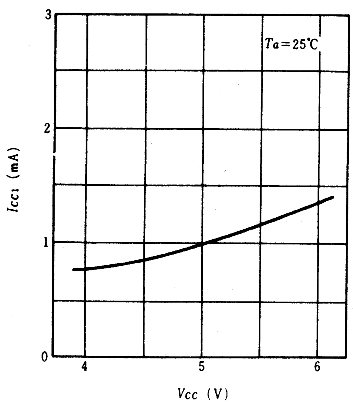
TYPICAL ACCESS TIME t_{CAC} vs. V_{CC}



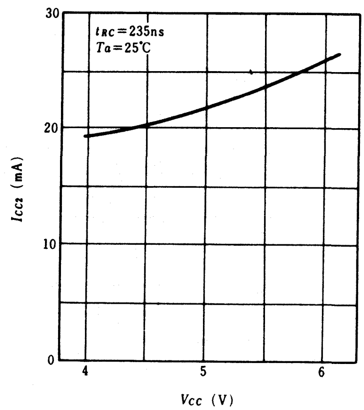
TYPICAL OPERATING CURRENT I_{CC2} vs. CYCLE RATE



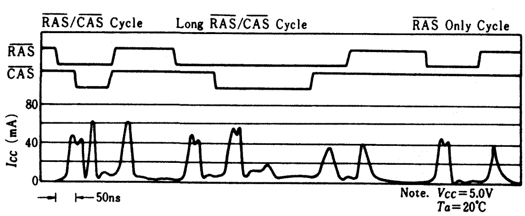
TYPICAL STANDBY CURRENT I_{CC1} vs. V_{CC}



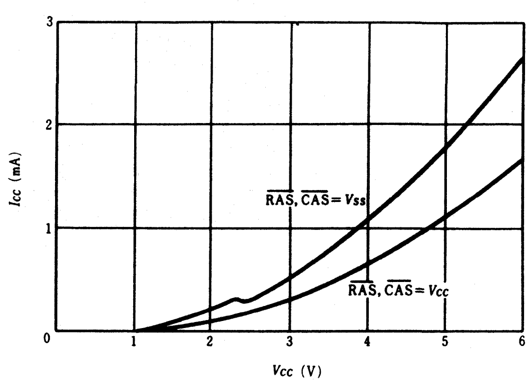
TYPICAL OPERATING CURRENT I_{CC2} vs. V_{CC}



● TYPICAL SUPPLY CURRENT WAVEFORMS



TYPICAL I_{CC} vs. V_{CC} DURING POWER UP



HM4864-2, HM4864-3
HM4864P-2, HM4864P-3

65536-word × 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

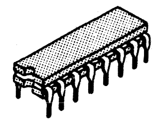
Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read,write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and $\overline{\text{RAS}}$-only refresh.

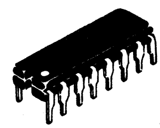
Proper control of the clock inputs ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

HM4864-2, HM4864-3



(DG-16A)

HM4864P-2, HM4864P-3

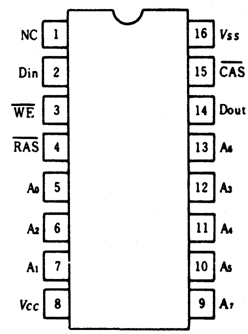


(DP-16)

■ FEATURES

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle time (HM4864-2, HM4864P-2)
- 200ns access time, 335ns cycle time (HM4864-3, HM4864P-3)
- Single power supply of +5V±10% with a built-in V_{BB} generator
- Low Power; 330 mW active. 20 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by $\overline{\text{CAS}}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{\text{RAS}}$-only refresh, and Page-mode capability
- 128 refresh cycle

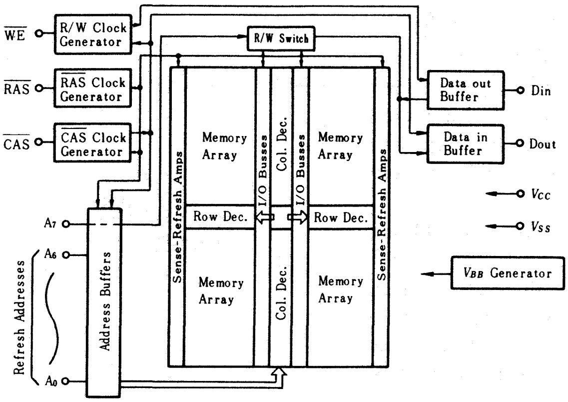
■ PIN ARRANGEMENT



(Top View)

A_0-A_7	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0-A_6	Refresh Address Strobe

■ FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . -1.0 to +7V
Operating Temperature, Ta (Ambient) . . . . 0 to +70°C
Storage Temperature (Ambient) . . . . -65 to +150°C
Short-circuit Output Current . 50 mA
Power Dissipation . . . . 1 W

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC}=min.)	I_{CC1}	—	60	mA	2, 4
STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = V_{IH}, Dout = High Impedance)	I_{CC2}	—	3.5	mA	2
REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}; t_{RC}=min.)	I_{CC3}	—	45	mA	2, 4
PAGE MODE CURRENT Average Power Supply Current, Page-mode Operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; t_{PC}=min.)	I_{CC4}	—	45	mA	2, 4
INPUT LEAKAGE Input Leakage Current, any Input (V_{in}=0 to +6.5V, all other pins not under test=0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE Output Leakage Current (Dout is disabled, V_{out}=0 to +5.5V)	I_{LO}	−10	10	μA	3
OUTPUT LEVELS Output High (Logic 1) Voltage (I_{out} = −5mA) Output Low (Logic 0) Voltage (I_{out} = 4.2mA)	V_{OH} V_{OL}	2.4 0	V_{CC} 0.4	V V	

NOTES
1. All voltages referenced to V_{SS}.
2. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
3. I_{LO} consists of leakage current only.
4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance (A_0-A_7, Din)	C_{in1}	—	7	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{in2}	—	10	pF	1
Output Capacitance (Dout)	C_{out}	—	7	pF	1, 2

NOTES
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [1), 2)]

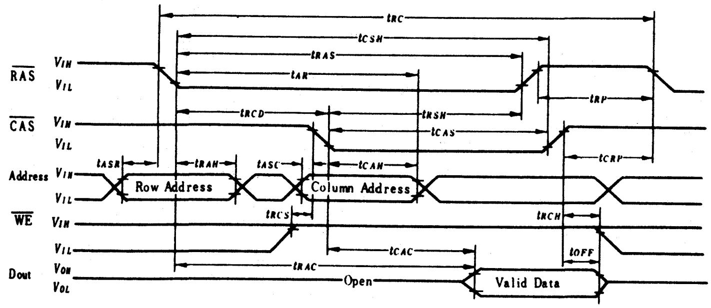
($Ta=0$ to $+70°C$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$)

Parameter	Symbol	HM4864-2/P-2		HM4864-3/P-3		Unit	Notes
		min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	270	—	335	—	ns	
Read-Write Cycle Time	t_{RWC}	270	—	335	—	ns	
Page Mode Cycle Time	t_{PC}	170	—	225	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	150	—	200	ns	4, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	100	—	135	ns	5, 6
Output Buffer Turn-off Delay	t_{OFF}	0	40	0	50	ns	7
Transition Time (Rise and Fall)	t_T	3	35	3	50	ns	3
$\overline{RAS}$ Precharge Time	t_{RP}	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	150	10000	200	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	—	135	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	—	135	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	—	200	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	25	65	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−20	—	−20	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	20	—	25	—	ns	
Column Address Set-up Time	t_{ASC}	−10	—	−10	—	ns	
Column Address Hold Time	t_{CAH}	45	—	55	—	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	95	—	120	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	95	—	120	—	ns	
Write Command Pulse Width	t_{WP}	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	45	—	55	—	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	95	—	120	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	60	—	80	—	ns	
Refresh Period	t_{REF}	—	2	—	2	ms	
Write Command Set-up Time	t_{WCS}	−20	—	−20	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60	—	80	—	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	110	—	145	—	ns	10
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	ns	

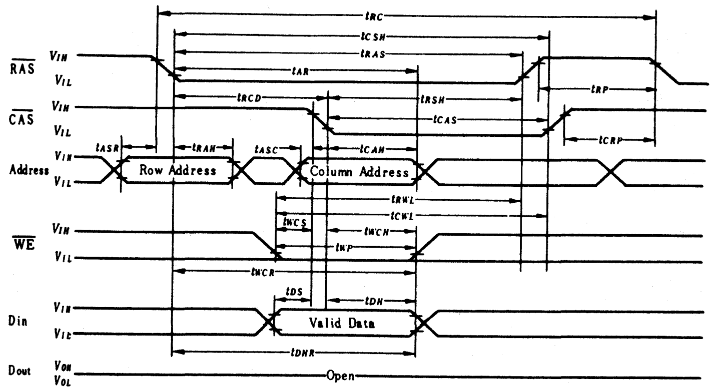
NOTES
1. AC measurements assume $t_T = 5$ns.
2. 8 cycles are required after power-on or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
9. These parameters are reference to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

■ TIMING WAVEFORMS

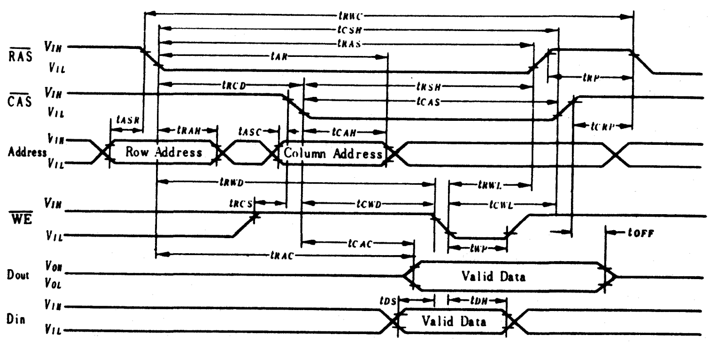
● READ CYCLE



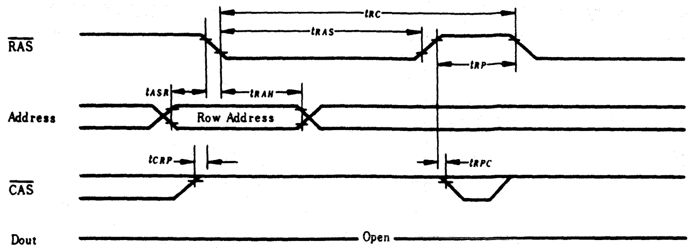
● WRITE CYCLE



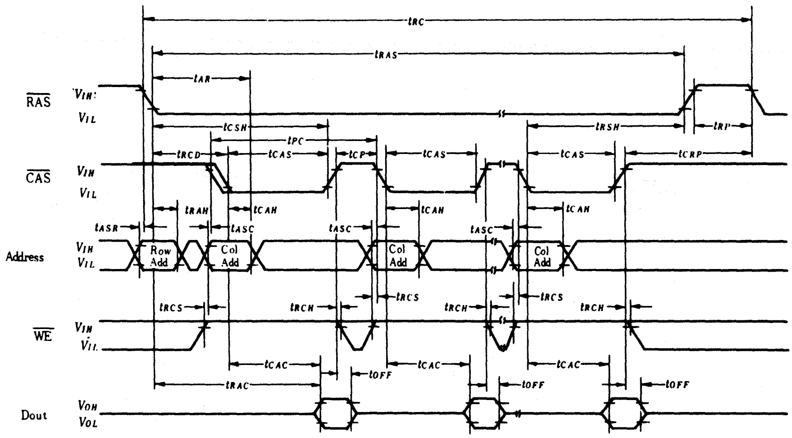
● READ-WRITE/READ-MODIFY-WRITE CYCLE



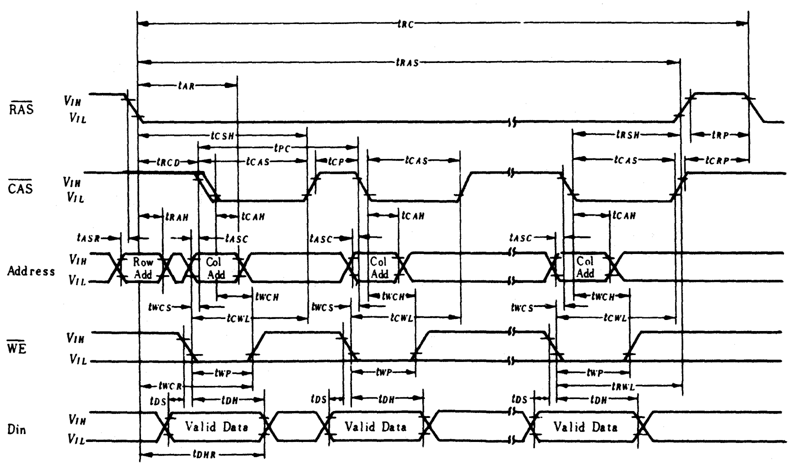
●"$\overline{RAS}$-ONLY" REFRESH CYCLE



●PAGE MODE READ CYCLE

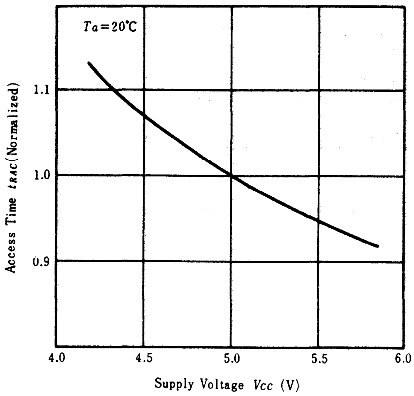


●PAGE MODE WRITE CYCLE

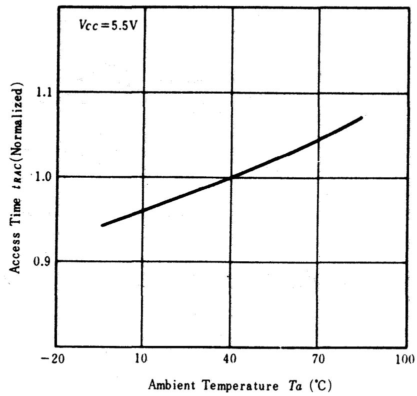


TYPICAL CHARACTERISTICS

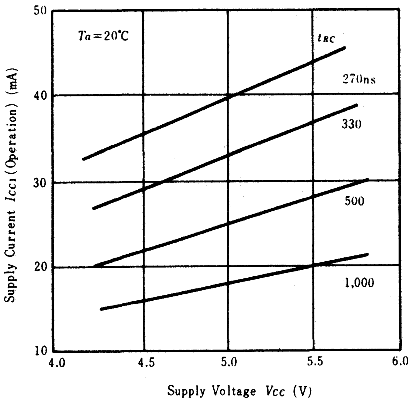
ACCESS TIME vs. SUPPLY VOLTAGE



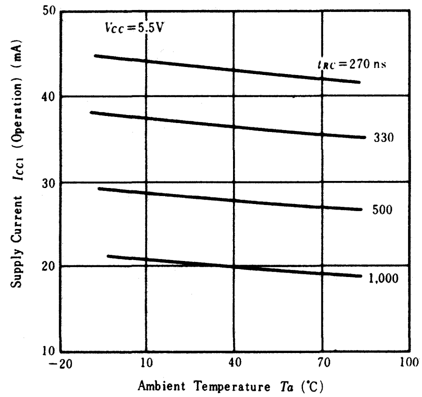
ACCESS TIME vs. AMBIENT TEMPERATURE



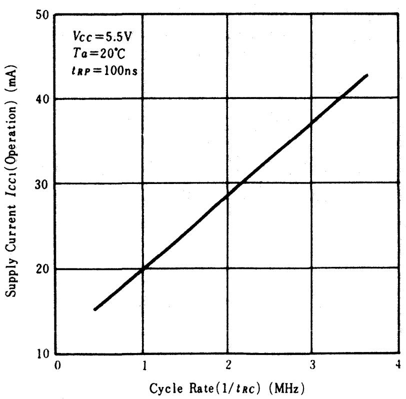
SUPPLY CURRENT vs. SUPPLY VOLTAGE



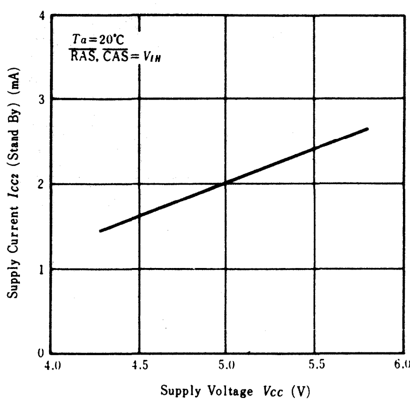
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



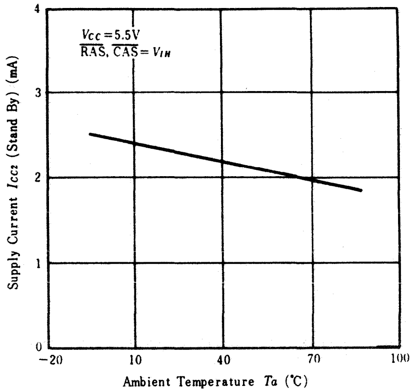
SUPPLY CURRENT vs. CYCLE RATE



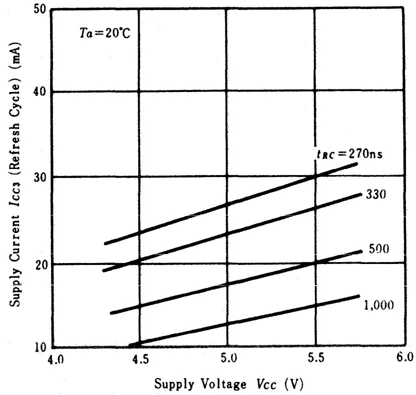
SUPPLY CURRENT vs. SUPPLY VOLTAGE



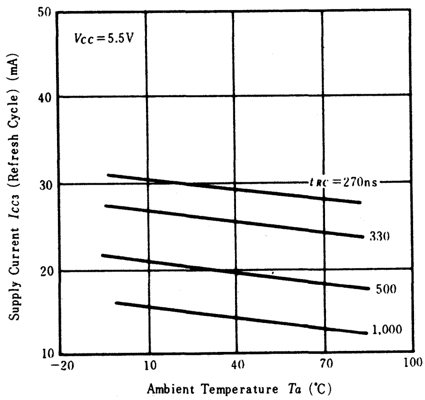
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



SUPPLY CURRENT
vs. SUPPLY VOLTAGE



SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



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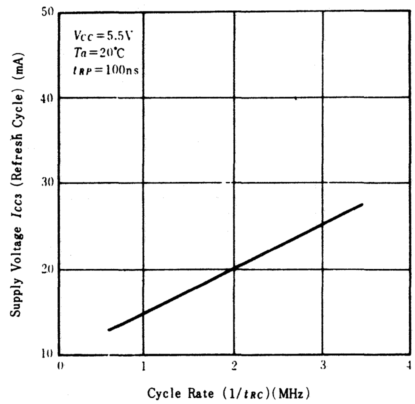
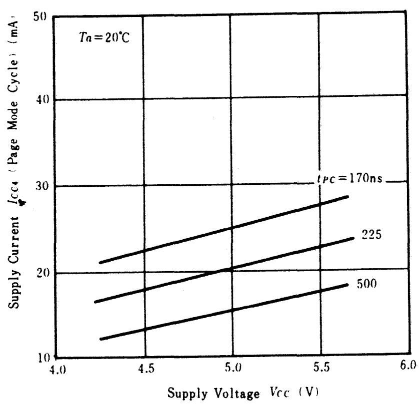
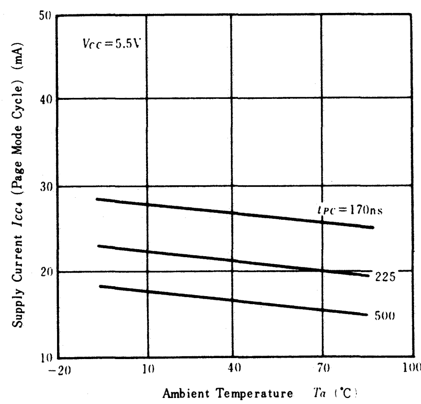
vs. CYCLE RATE



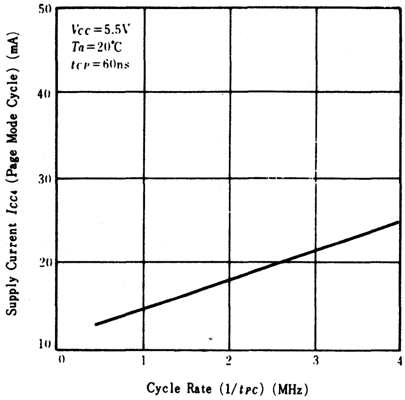
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



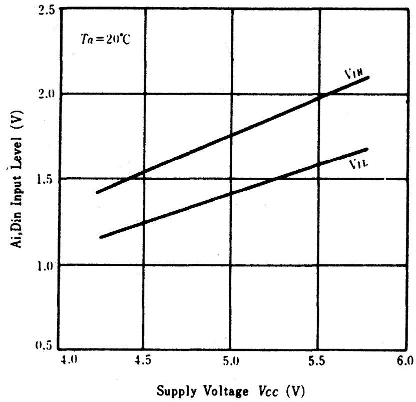
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



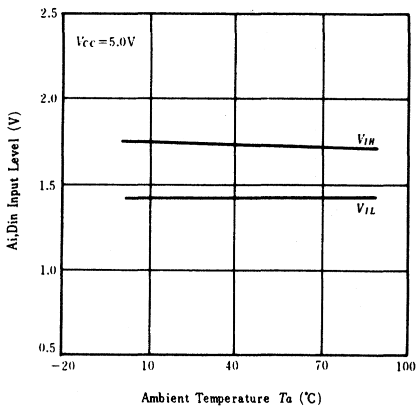
SUPPLY CURRENT vs. CYCLE RATE



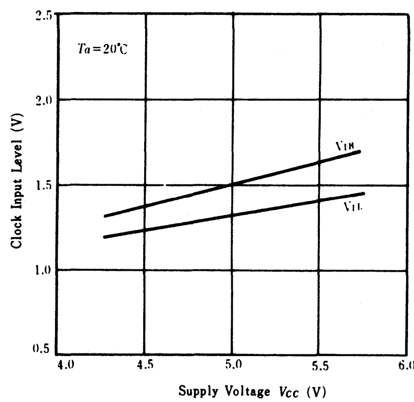
INPUT LEVEL vs. SUPPLY VOLTAGE



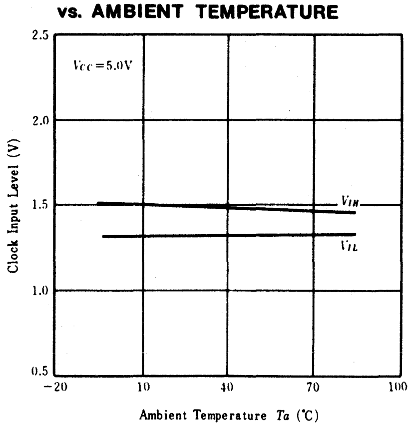
INPUT LEVEL vs. AMBIENT TEMPERATURE

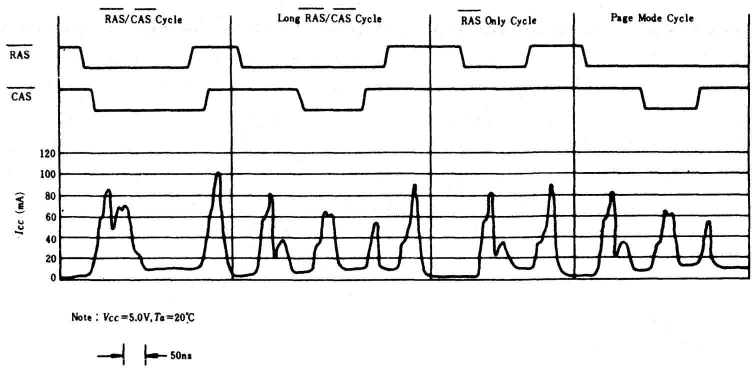


CLOCK INPUT LEVEL vs. SUPPLY VOLTAGE



CLOCK INPUT LEVEL vs. AMBIENT TEMPERATURE





■APPLICATION INFORMATION

●POWER ON

An initial pause of 500 μs is required after power-up and a minimum of eight (8) initialization cycle,(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh) must follow an initial pause.

The V_{CC} current (I_{CC}) requirement of the HM4864 during power on is, however, dependent upon the input levels ($\overline{RAS}$, $\overline{CAS}$) and the rise time of V_{CC}, as shown in Fig. 1.

●READ CYCLE

A read cycle begins with addresses stable and a negative going transition of $\overline{RAS}$. The time delay between the stable address and the start of $\overline{RAS}$-on is controlled by parameter t_{ASR}.

Following the time when $\overline{RAS}$ reaches its low level, the row address must be held stable long enough to be captured. This controlling parameter is t_{RAH}. Following this interval, the address can be changed from row address to column address. When the column address is stable, $\overline{CAS}$ can be turned on. The leading edge of $\overline{CAS}$ is controlled by parameter t_{RCD}. The basic limit on the $\overline{CAS}$ leading edge is that $\overline{CAS}$ can not start until the column address is stable, and this is controlled by parameter t_{ASC}. The column address must be held stable long enough to be captured. The controlling parameter is t_{CAH}. Note that t_{RCD} (max) is not an operating limit of the HM4864 though its specification is listed on the data sheets. If $\overline{CAS}$ becomes on later than t_{RCD} (max), the access time from $\overline{RAS}$ will be increased by the time which t_{RCD} exceeds t_{RCD} (max).

Following the time when $\overline{CAS}$ reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is t_{CAC} -access time from $\overline{CAS}$.

The access time from $\overline{RAS}$—t_{RAC}—is the time from $\overline{RAS}$-on to valid Dout.

The minimum value of t_{RAC} is derived as the sum of t_{RCD} (max) and t_{CAC}.

The selected output data is held valid internally until $\overline{CAS}$ becomes high, and then Dout pin becomes high impedance. This parameter is t_{OFF}.

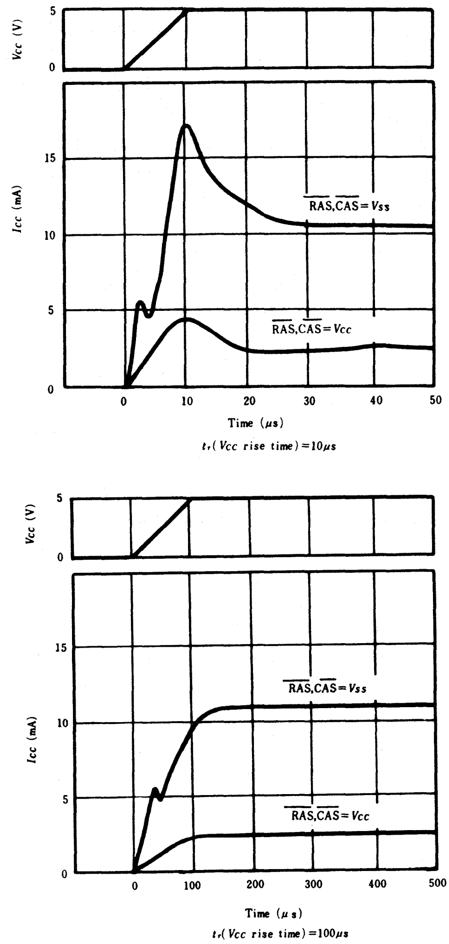


Fig.1 I_{CC} vs. V_{CC} during power up.

• WRITE CYCLE

A write cycle is performed by bringing $\overline{WE}$ low before or during $\overline{CAS}$-on.

Two different write cycles can be defined as;

Write cycle—Write data are available at the beginning of the $\overline{CAS}$-on so that the write operation starts at the beginning. In this mode, Dout and $\overline{WE}$ signal times are not in any critical path for determining cycle time.

Following the time when $\overline{WE}$ reaches its low level, $\overline{WE}$ must be held stable long enough to be captured. This $\overline{WE}$-on pulse deration is called t_{WP}. The time required to capture write data in a latch is called t_{DH}. This cycle is called an "early write".

Read Write cycle—This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated.

$\overline{WE}$ and Din are delayed until after Dout. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, Din and $\overline{WE}$ become critical path signals for determining cycle time.

• CLOCK-OFF TIMING

$\overline{RAS}$ and $\overline{CAS}$ must stay on for Dout stabilized to valid data. In the case of $\overline{CAS}$, this is controlled by parameter t_{CAS} (min).

In the case of $\overline{RAS}$, this is controlled by parameter t_{CAS} (min). Following the end of $\overline{RAS}$, $\overline{CAS}$ must stay off long enough to precharge internal circuits. The only parameter of concern is t_{RP}. Normally $\overline{CAS}$ is not required to be off for minimum time of t_{CRP}. However, in a page mode memory operation, there is a t_{CP} (min) specification to control the $\overline{CAS}$-off time.

• DATA OUTPUT

Dout is three-state TTL compatible with a fan-out of two standard TTL loads.

When $\overline{CAS}$ is high, Dout is in a high impedance state. When $\overline{CAS}$ is low, valid data appears after t_{CAC} at a read cycle, and Dout is not valid as an early-write cycle.

• REFRESH

Refresh of the HM4864 is accomplished by performing a memory cycle at each of the 128 row addresses within each two millisecond time interval. A0 to A6 are refresh address pin compatible with standard 16K RAM (HM4716A, HM4816A). During refresh, either V_{IL} or V_{IH} is permitted for A7. Any cycle in which $\overline{RAS}$ signal occurs refreshes the entire selected row. $\overline{RAS}$-only refresh results in substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

• PAGE MODE

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining $\overline{RAS}$ at a logic low throughout all successive $\overline{CAS}$ memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be descreaded and the operating power is reduced. These are specifications.

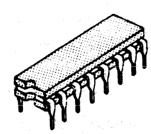
HM4864A-12, HM4864A-15, HM4864A-20, HM4864AP-12, HM4864AP-15, HM4864AP-20 —Preliminary—

65536-word × 1-bit Dynamic Random Access Memory

■ FEATURES

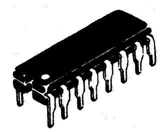
- Industry standard 16- Pin DIP (plastic, Cerdip)
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 275 mW active, 20 mW standby
- High speed: Access Time 120ns / 150ns / 200ns
- Common I/O capability using early write operation
- Page mode capability
- Output data controlled by $\overline{CAS}$
- TTL compatible
- 128 refresh cycles – (2ms)

HM4864A-12, HM4864A-15, HM4864A-20



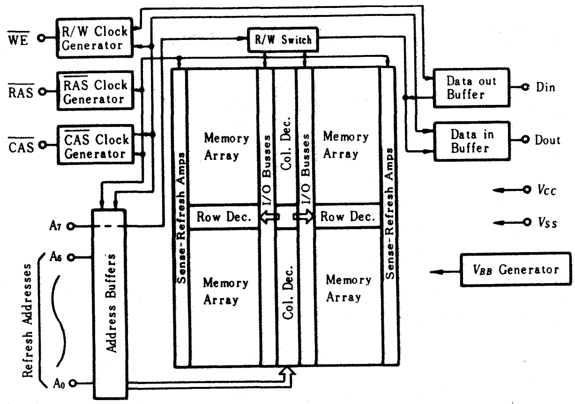
(DG-16B)

HM4864AP-12, HM4864AP-15, HM4864AP-20

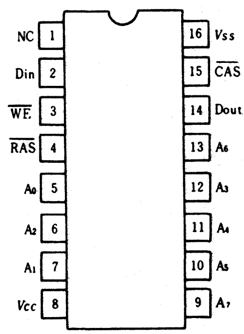


(DP-16)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

A0–A7	:	Address Inputs
$\overline{CAS}$	:	Column Address Strobe
Din	:	Data In
Dout	:	Data Output
$\overline{RAS}$	:	Row Address Strobe
$\overline{WE}$	:	Read/Write Input
V_{CC}	:	Power (+5V)
V_{SS}	:	Ground
A0–A6	:	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ·············· –1V to 7V
Operating temperature, Ta (Ambient) ·········· 0°C to 70°C
Storage temperature (Cerdip) ·················· –65°C to 150°C
Storage temperature (Plastic) ················· –55°C to 125°C
Power dissipation ···························· 1 W
Short circuit output current ················· 50 mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to 70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage	V_{IL}	–1.0	–	0.8	V	1

Notes : 1. All voltages referenced to V_{SS}

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ DC ELECTRICAL CHARACTERISTICS (Ta=0 to 70℃, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	min	max	Unit	Notes
Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling : t_{RC}=min)	I_{CC1}	—	50	mA	1, 2
Standby Current ($\overline{RAS}=V_{IH}$, Dout=High Impedance)	I_{CC2}	—	3.5	mA	
Refresh Current ($\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$, t_{RC}=min)	I_{CC3}	—	35	mA	2
Standby Current ($\overline{RAS}=V_{IH}$, Dout Enable)	I_{CC5}	—	5.5	mA	1
Page Mode Current ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Cycling; t_{PC}=min)	I_{CC6}	—	35	mA	1, 2
Input Leakage ($0<V_{out}<6.5V$)	I_{LI}	−10	10	μA	
Output Leakage (Dout is disabled, $0<V_{out}<5.5V$)	I_{LO}	−10	10	μA	
Output Levels High (I_{out}=−5mA)/Low (I_{out}=4.2mA)	V_{OH}, V_{OL}	2.4/0	V_{CC}/0.4	V/V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

■ CAPACITANCE (V_{CC}=5V±10%, Ta=25℃)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	$A_0 \sim A_7$, Din	C_{in1}	—	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{in2}	—	10	pF	1
Output Capacitance	Dout	C_{out}	—	7	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}=V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Ta=0 to 70℃, V_{CC}=5V±10%, V_{SS}=0V)

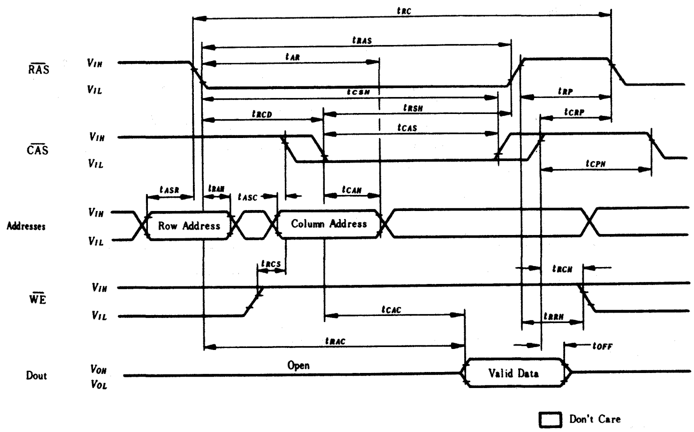
Parameter	Symbol	HM4864A-12		HM4864A-15		HM4864A-20		Unit	Notes
		min	max	min	max	min	max		
Access Time From $\overline{RAS}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time From $\overline{CAS}$	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	35	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	35	3	35	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	230	—	260	—	330	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	100	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	2ms	75	2ms	100	2ms	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	−10	—	−10	—	−10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	80	—	100	—	130	—	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	9
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	2	—	2	—	2	ms	
Read-Write Cycle Time	t_{RWC}	255	—	280	—	345	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	40	—	45	—	55	—	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	100	—	120	—	155	—	ns	
Page Mode Cycle Time	t_{PC}	130	—	145	—	190	—	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	60	—	60	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	30	—	35	—	45	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

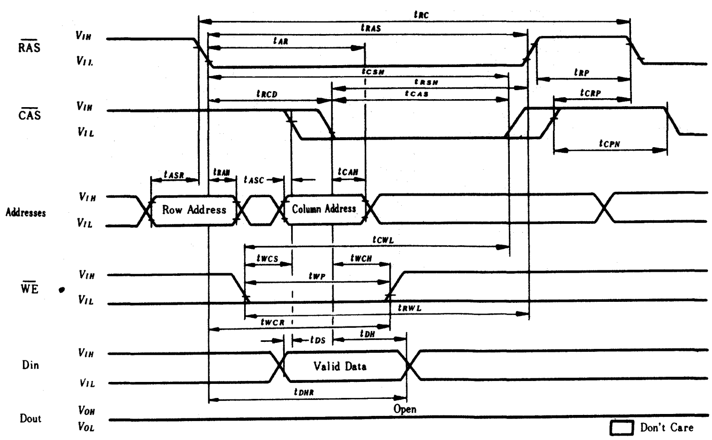
1. AC measurements assume $t_T = 5$ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet is electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. There parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge is delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■TIMING WAVEFORMS

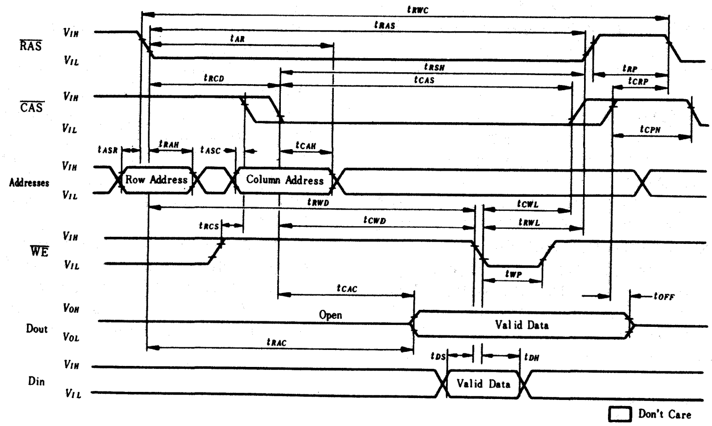
●READ CYCLE



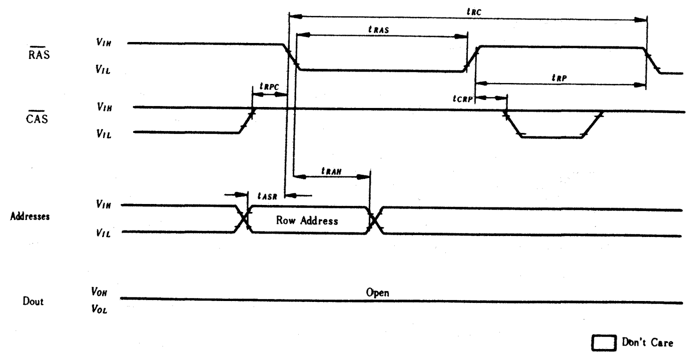
●WRITE CYCLE (EARLY WRITE)



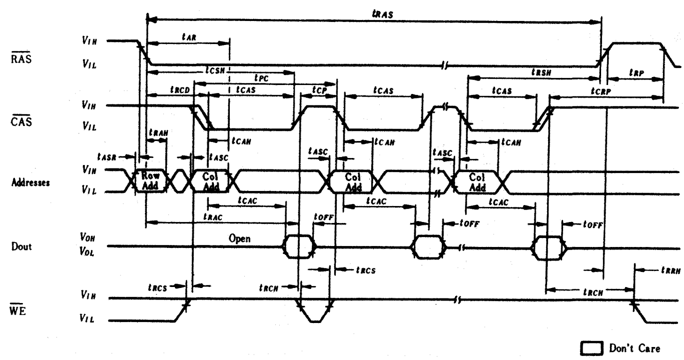
● READ-WRITE/READ-MODIFY-WRITE CYCLE



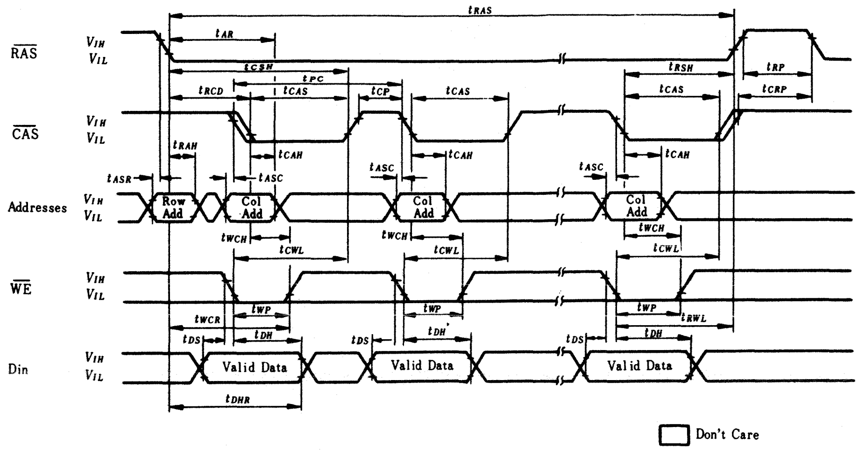
● "RAS-ONLY" REFRESH CYCLE



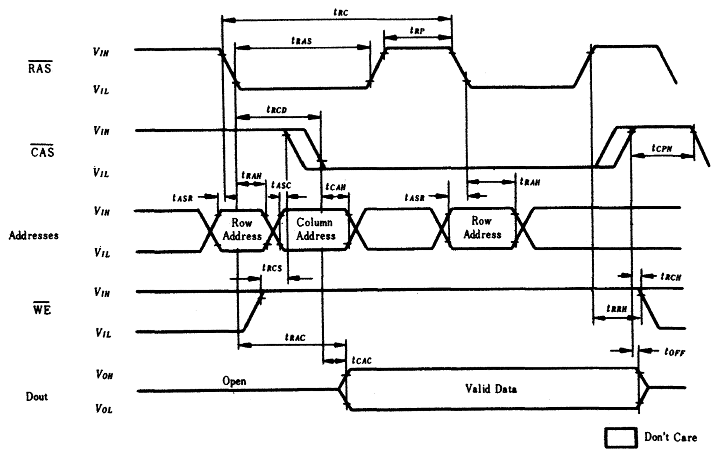
● PAGE MODE READ CYCLE



●PAGE MODE WRITE CYCLE



●HIDDEN REFRESH CYCLE



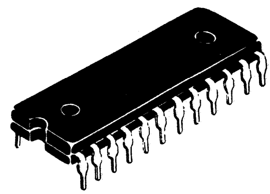
MOS ROM

HN46332P

4096-word × 8-bit Mask Programmable Read Only Memory

The HN46332P is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL and DTL, and requires no clocks or refreshing because of static operation.

The memory is compatible with the HMCS6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

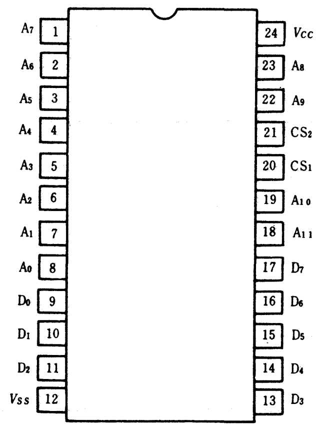


(DP-24)

■ FEATURES

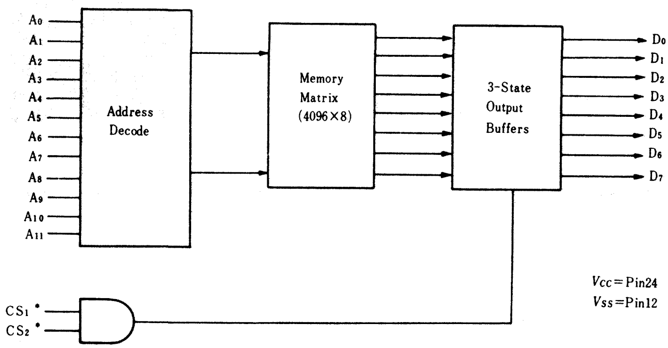
- Fully Static operation
- Three-State Data Output for OR-Ties
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single + 5-Volt Power Supply
- Fully TTL Compatible
- Maximum Access Time = 350ns
- N-Channel Si Gate MOS Technology
- Pin Compatible with EPROMs

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



* Active level defined by the user.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	℃
Storage Temperature Range	T_{stg}	−55 to +125	℃

* With respect to V_{SS}.

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.0	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	℃

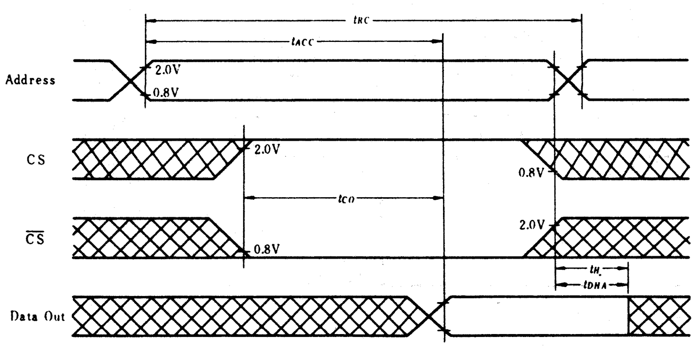
■ ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75°C unless otherwise noted)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input High-level Voltage	V_{IH}		2.0	—	V_{CC}	V
Input Low-level Voltage	V_{IL}		−0.3	—	0.8	V
Output High-level Voltage	V_{OH}	I_{OH}=−100 μA	2.4	—	—	V
Output Low-level Voltage	V_{OL}	I_{OL}=1.6mA	—	—	0.4	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5V	—	—	2.5	μA
Output High-level Leakage Current	I_{LOH}	V_{out}=2.4V, CS=0.8V, $\overline{CS}$=2.0V	—	—	10	μA
Output Low-level Leakage Current	I_{LOL}	V_{out}=0.4V, CS=0.8V, $\overline{CS}$=2.0V	—	—	10	μA
Supply Current	I_{CC}	V_{CC}=5.5V	—	—	80	mA
Input Capacitance	C_{in}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	7.5	pF
Output Capacitance	C_{out}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	12.5	pF

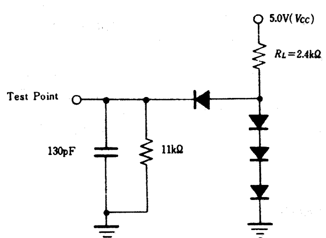
■ AC OPERATING CONDITIONS AND CHARACTERISTICS

● READ SEQUENCE

Item	Symbol	min.	max.	Unit
Read Cycle Time	t_{RC}	350	—	ns
Address Access Time	t_{ACC}	—	350	ns
Chip Enable to Output Time	t_{CO}	—	150	ns
Data Hold Time from Address	t_{DHA}	10	—	ns
Data Hold Time from Deselection	t_H	10	150	ns



■ AC TEST LOAD



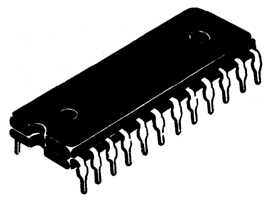
Notes : 1. $t_r=t_f$=20ns
2. C_L includes jig capacitance
3. All diodes are 1S2074 Ⓗ

HN48364P

8192-word × 8-bit Mask Programmable Read Only Memory

The HN48364P is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL and DTL, and requires no clocks or refreshing because of static operation.

The memory is compatible with the HMCS6800 Microcomputer Family, providing read only storage in byte increments. The active level of the Chip Enable input and the memory content are defined by the user. The Chip Enable input deselects the output and puts the chip in a power down mode.

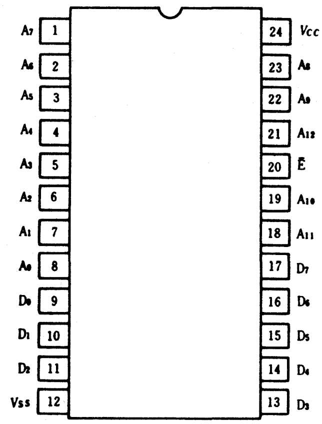


(DP-24)

■ FEATURES

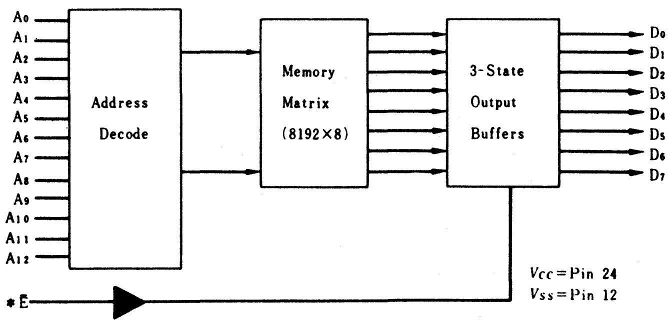
- Fully Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Enable
- TTL Compatible
- Maximum Access Time-350ns
- Pin Compatible with EPROMs

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



*Active level defined by the user

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

* With respect to V_{SS}.

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.0	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	C

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75°C unless otherwise noted.)

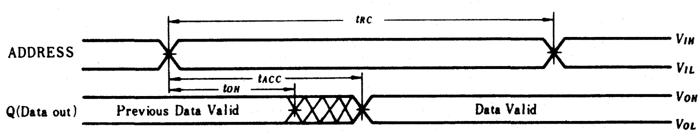
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input High-level Voltage	V_{IH}	—	2.0	—	V_{CC}	V
Input Low-level Voltage	V_{IL}	—	−0.3	—	0.8	V
Output High-level Voltage	V_{OH}	I_{OH}=−205μA	2.4	—	—	V
Output Low-level Voltage	V_{OL}	I_{OL}=3.2mA	—	—	0.4	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5V	—	—	2.5	μA
Output High-level Leakage Current	I_{LOH}	V_{out}=2.4V, E=0.8V, $\overline{E}$=2.0V	—	—	10	μA
Output Low-level Leakage Current	I_{LOL}	V_{out}=0.4V, E=0.8V, $\overline{E}$=2.0V	—	—	10	μA
Supply Current (Active/Standby)	I_{CC}/I_{sb}	V_{CC}=5.5V	—	45/6	80/10	mA
Input Capacitance	C_{in}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	7.5	pF
Output Capacitance	C_{out}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	12.5	pF

■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

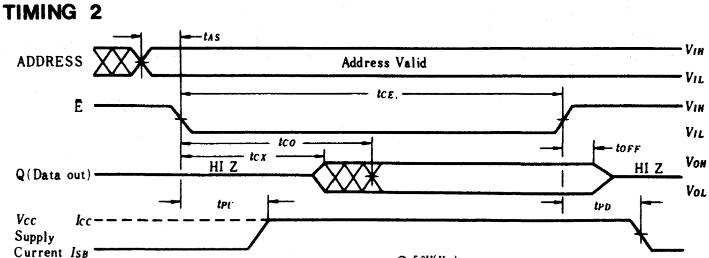
(V_{CC}=5.0V±10%, Ta=−20 to +75°C, All timing with $t_r=t_f$=20ns)

Item	Symbol	min.	max.	Unit
Read Cycle Time	t_{RC}	350	—	ns
Chip Enable Pulse Width	t_{CE}	350	—	ns
Address Access Time	t_{ACC}	—	350	ns
Chip Enable to Output Time	t_{CO}	—	350	ns
Previous Read Data Valid	t_{OH}	10	—	ns
Chip Enable Low to Output Invalid	t_{CX}	10	—	ns
Chip Enable High to Output High Z	t_{OFF}	0	80	ns
Chip Selection to Power Up Time	t_{PU}	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	120	ns
Address Setup Time	t_{AS}	0	—	ns

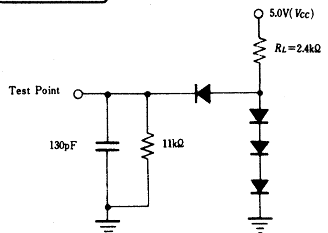
● READ CYCLE TIMING 1 ($\overline{E}$ Held Low)



● READ CYCLE TIMING 2



■ AC TEST LOAD

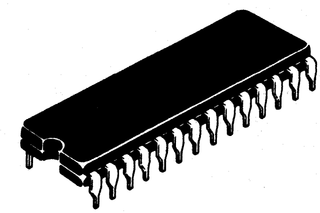


Notes : 1. $t_r=t_f$=20ns
2. C_L includes jig capacitance
3. All diodes are 1S2074Ⓗ

HN43128P

16384 × 8-bit or 32768 × 4-bit CMOS Mask Programmable Read Only Memory

The Hitachi HN43128P is a mask programmable, 16384x8-bit or 32786x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL and DTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through two chip select inputs. Either active "High" or active "Low" of chip select inputs and a chip enable input is defined at mask level. The organization of 8 bit or 4 bit is designed by the user.

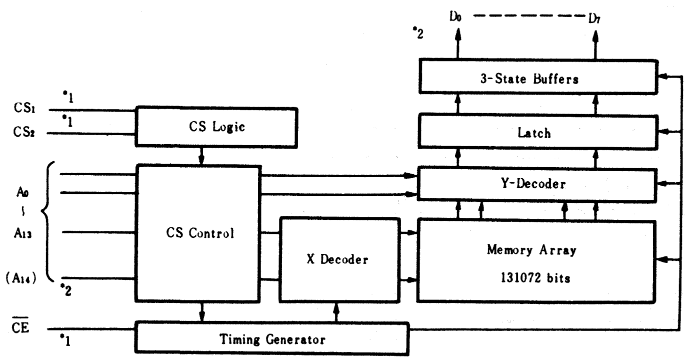


(DP-28)

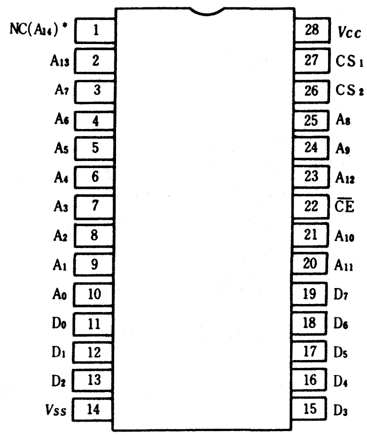
■ FEATURES

- Mask-programmable for either 4-bit or 8-bit organization.
- Three-state outputs, can be wired-OR.
- Two mask programmable chip select terminals facilitate memory expansion.
- A signle 5V power supply (±10%).
- Low power consumption: 3mW typ.
- TTL compatible
- Access time: 6μs (max)
- Si gate CMOS technology

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

* The most significant address in 4-bit organization.

■ PIN EXPLANATION

A_0-A_{14}	Address Inputs
D_0-D_7	Data Outputs
CS_1, CS_2	Chip Select Inputs
$\overline{CE}$	Chip Enable Input
V_{CC}	+5V
V_{SS}	GND

*1 Active level defined at mask level.
*2 Mask programmable selection of either 4-bit or 8-bit organization.
In 4-bit organization, data outputs are D_0 to D_3.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{CC}	−0.3〜+7.0	V
Input Voltage*	V_{in}	−0.3〜+7.0	V
Operating Temperature Range	T_{opr}	−20〜+75	℃
Storage Temperature	T_{stg}	−55〜+125	℃

Note : * Referenced to V_{SS}.

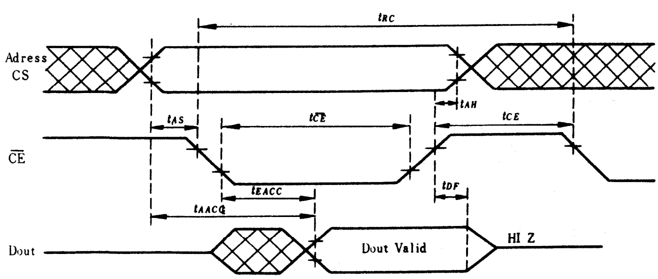
■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC}=5V±10%, V_{SS}=0V, Ta=−20〜+75℃)

Item		Symbol	Test Condition		min	typ	max	Unit
Input "High" Level Voltage		V_{IH}			2.4	—	V_{CC}	V
Input "Low" Level Voltage		V_{IL}			0	—	0.8	V
Output "High" Level Voltage		V_{OH}	$I_{OH}=-100\mu A$		2.4	—	—	V
Output "Low" Level Voltage		V_{OL}	$I_{OL}=1.6mA$		—	—	0.4	V
Input Leakage Current		I_{in}	$V_{in}=0\sim5.5V$		—	—	2.0	μA
Output "High" Level Leakage Current		I_{LOH}	CE=0.8V	$V_{out}=2.4V$	—	—	5	μA
Output "Low" Level Leakage Current		I_{LOL}	$\overline{CE}$=2.0V	$V_{out}=0.4V$	—	—	5	μA
Supply Current	In stand-by	I_{SB}	$V_{IH}\geqq V_{CC}-0.2V$, $V_{IL}\leqq V_{SS}+0.2V$	$V_{CC}=5V$	—	1	50	μA
	In operation	I_{CC}	$t_{RC}=7.5\mu s$		—	0.6	1.5	mA
Input Capacitance		C_{in}	$V_{in}=0V, f=1MHz, Ta=25℃$		—	—	10	pF
Output Capacitance		C_{out}			—	—	12.5	pF

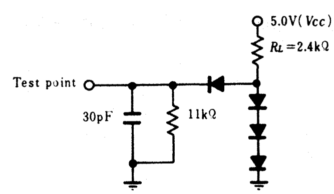
■ AC OPERATING CHARACTERISTICS

● READ SEQUENCE

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	7.5	—	μs
Address Access Time	t_{AACC}	—	6.5	μs
Chip Enable Access Time	t_{EACC}	—	6.0	μs
Data Hold Time from Address	t_{DF}	0.05	0.5	μs
Address Set-up Time	t_{AS}	0.5	—	μs
Address Hold Time	t_{AH}	0	—	μs
Chip Enable ON Time	$t_{\overline{CE}}$	6.0	—	μs
Chip Enable OFF Time	t_{CE}	1.0	—	μs



● LOAD CIRCUIT

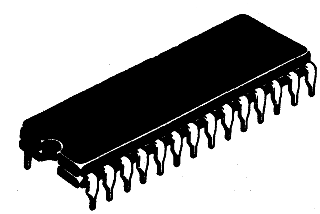


Notes : 1. $t_r=t_f=20ns$.
2. C_L includes jig capacitance.
3. All diodes are 1S2074 Ⓗ.

HN613128P

16384-word × 8-bit Mask Programmable Read Only Memory

The HN613128P is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL and DTL, and requires no clocks or refreshing because of static operation. The active level of the $\overline{CS}$, $\overline{OE_0}$, $\overline{OE_1}$ input and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

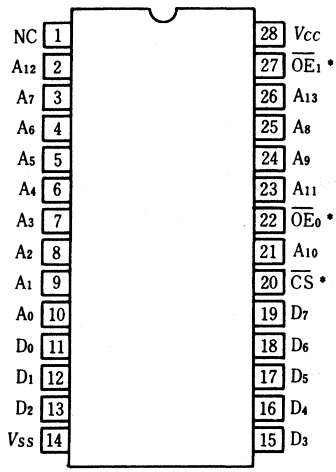


(DP-28)

■ FEATURES

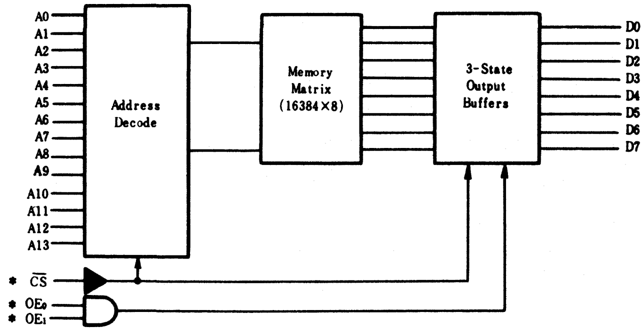
- Fully Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select, Output Enable
- TTL Compatible
- Maximum Access Time-250ns
- Low Power Standby and Low Power Operation;
  - Standby: 5μW (typ.)
  - Operation: 100mW (typ.)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



* Active level defined by the user.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

* With respect to V_{SS}.

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	−0.3	−	0.8	V
	V_{IH}	2.0	−	V_{CC}	V
Operating Temperature	T_{opr}	−20	−	75	°C

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75°C unless otherwise noted)

Item	Symbol	Test Condition	min	typ	max	Unit
Input High-level Voltage	V_{IH}		2.0	—	V_{CC}	V
Input Low-level Voltage	V_{IL}		−0.3	—	0.8	V
Output High-level Voltage	V_{OH}	$I_{OH}=-205\mu A$	2.4	—	—	V
Output Low-level Voltage	V_{OL}	I_{OL}=3.2mA	—	—	0.4	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5V	—	—	2.5	μA
Output High-level Leakage Current	I_{LOH}	V_{out}=2.4V, CS=0.8V, $\overline{CS}$=2.0V	—	—	10	μA
Output Low-level Leakage Current	I_{LOL}	V_{out}=0.4V, CS=0.8V, $\overline{CS}$=2.0V	—	—	10	μA
Supply Current (Active/Standby)	I_{CC}/I_{sb}	V_{CC}=5.5V, I_{DOUT}=0mA /$\overline{CS}\geq V_{CC}-0.2$V, CS≦0.2V	—	20/1	40/30	mA/μA
Input Capacitance	C_{in}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	10	pF
Output Capacitance	C_{out}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	15	pF

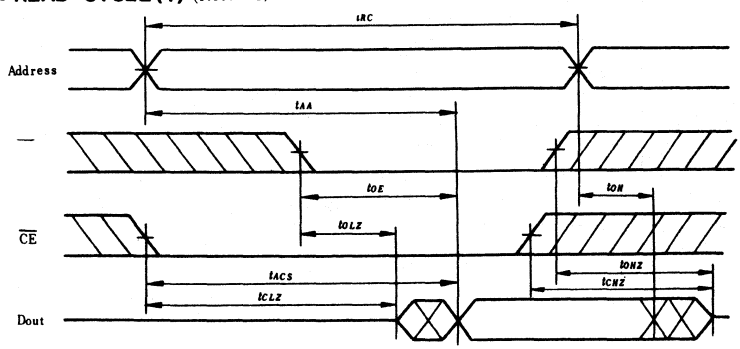
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5.0V±10%, Ta=−20 to +75°C, All timing with $t_r=t_f$=20ns)

Item	Symbol	HN613128P		Unit
		min	max	
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	80	ns
Chip Disable to Output in High Z	t_{OHZ}	0	80	ns
Output Hold from Address Change	t_{OH}	10	—	ns

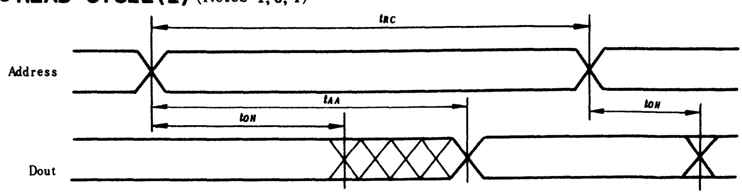
■ TIMING WAVEFORM

● READ CYCLE (1) (Notes 4)

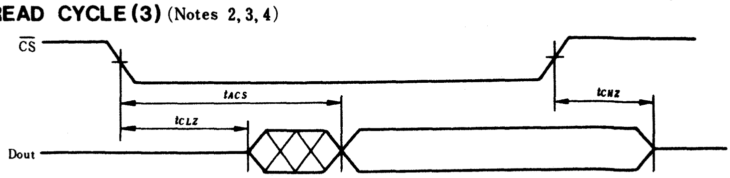


NOTES:
1. Device is continuously selected.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = VIL.
4. When $\overline{CS}$ is Low, the address input must be in the high impedance state.

● READ CYCLE (2) (Notes 1, 3, 4)



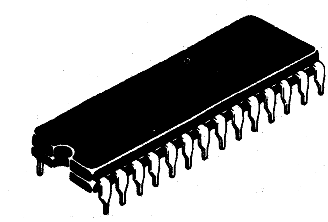
● READ CYCLE (3) (Notes 2, 3, 4)



HN61256P

32768 × 8-bit or 65536 × 4-bit CMOS Mask Programmable Read Only Memory

The Hitachi HN61256P is a mask programmable, 32768x8-bit or 65536x4-bit CMOS read only memory. It operates from a single power supply and is compatibel with TTL and DTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through one chip select input. Either active "High" or active "Low" or chip select input and a chip enable input are defined at mask level. The organization of 8 bit or 4 bit is defined by the user.

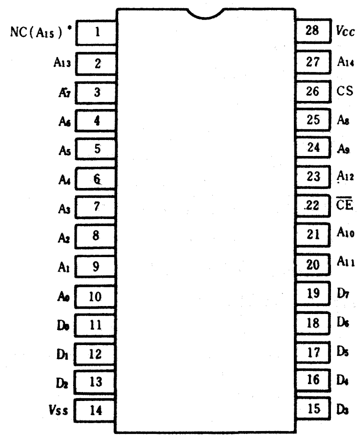


(DP-28)

■ FEATURES

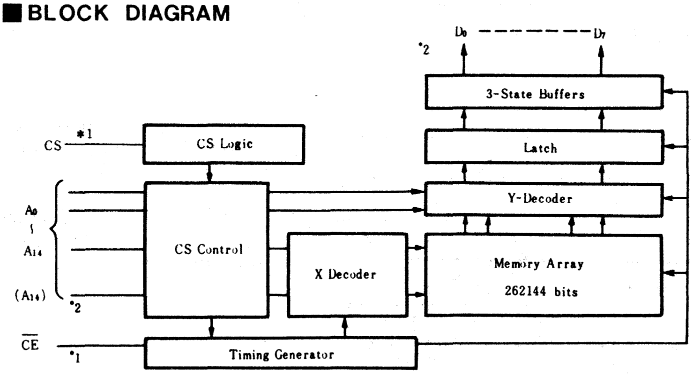
- Mask-programmable selection of either 4-bit or 8-bit organization.
- Three-state outputs, can be wire-ORed.
- One mask programmable chip select terminal facilitates memory expansion.
- A single 5V power supply (±10%).
- Low power consumption: 7.5mW typ.
- TTL compatible
- Access time: 3μs (max)
- Si gate CMOS technology

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ PIN EXPLANATION

A_0 - A_{15}	Address Inputs
D_0 - D_7	Data Outputs
CS	Chip Select Input
$\overline{CE}$	Chip Enable Input
V_{CC}	+5V
V_{SS}	GND

*1 Active level defined at mask level.
*2 Mask programmable selection of either 4-bit or 8-bit organization.
In 4-bit organization, data outputs are D_0 to D_3.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{CC}	−0.3∼+7.0	V
Input Voltage*	V_{in}	−0.3∼+7.0	V
Operating Temperature Range	T_{opr}	−20∼+75	℃
Storage Temperature Range	T_{stg}	−55∼+125	℃

Note : * Referenced to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

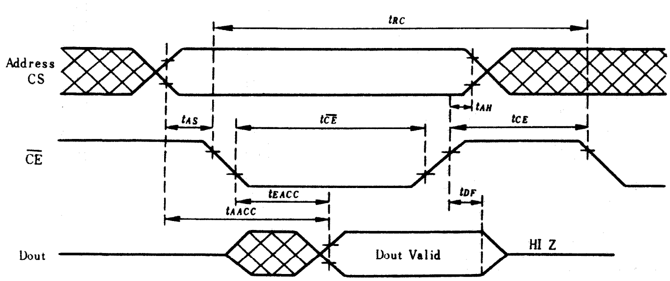
(Unless otherwise specified, V_{CC}=5V±10%, V_{SS}=0V, Ta=−20∼+75℃)

Item		Symbol	Test Condition		min	typ	max	Unit
Input "High" Level Voltage		V_{IH}			2.4	—	V_{CC}	V
Input "Low" Level Voltage		V_{IL}			0	—	0.8	V
Output "High" Level Voltage		V_{OH}	I_{OH}=−100μA		2.4	—	—	V
Output "Low" Level Voltage		V_{OL}	I_{OL}=1.6mA		—	—	0.4	V
Input Leakage Current		I_{in}	V_{in}=0∼5.5V		—	—	2.0	μA
Output "High" Level Leakage Current		I_{LOH}	CE=0.8V	V_{out}=2.4V	—	—	5	μA
Output "Low" Level Leakage Current		I_{LOL}	$\overline{CE}$=2.0V	V_{out}=0.4V	—	—	5	μA
Supply Current	In stand-by	I_{SB}	CS≧V_{CC}−0.2V, CS≦V_{SS}+0.2V	V_{CC}=5V	—	1	50	μA
	In operation	I_{CC}	t_{RC}=4.0μs		—	1.5	3.0	mA
Input Capacitance		C_{in}	V_{in}=0V, f=1MHz, Ta=25℃		—	—	10	pF
Output Capacitance		C_{out}			—	—	12.5	pF

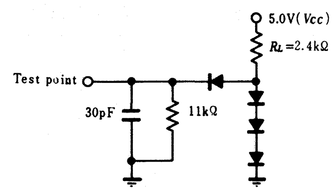
■ AC OPERATING CONDITION AND CHARACTERISTICS

● READ SEQUENCE

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	4.0	—	μs
Address Access Time	t_{AACC}	—	3.5	μs
Chip Enable Access Time	t_{EACC}	—	3.0	μs
Data Hold Time from Address	t_{DF}	0.05	0.5	μs
Address Set-up Time	t_{AS}	0.5	—	μs
Address Hold Time	t_{AH}	0	—	μs
Chip Enable ON Time	$t_{\overline{CE}}$	3.0	—	μs
Chip Enable OFF Time	t_{CE}	0.5	—	μs



● LOAD CIRCUIT



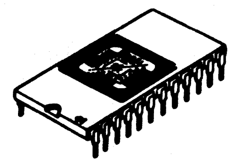
Notes : 1. $t_r = t_f$ = 20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

HN462716, HN462716G

2048-word × 8-bit U.V. Erasable and Electrically Programmable Read Only Memory

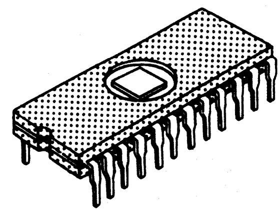
The HN462716 is a 2048 word by 8 bit erasable and electrically programmable ROMs. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

HN462716



(DC-24C)

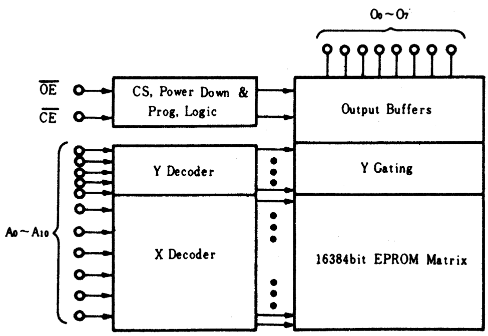
HN462716G



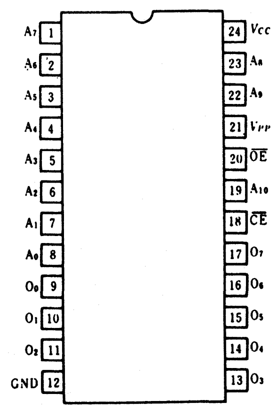
(DG-24B)

- Single Power Supply ···· +5V ±5%
- Simple Programming ···· Program Voltage: +25V DC
  Programs with One 50ms Pulse
- Static ················ No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded-on Chip Address Decode
- Access Time ········· 450ns Max.
- Low Power Dissipation ·· 555mW Max. Active Power
  213mW Max. Standby Power
- Three State Output ····· OR- Tie Capability
- Interchangeable with Intel 2716

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PROGRAMMING OPERATION

Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5	+5	Dout
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	Din
Program Verify	V_{IL}	V_{IL}	+25	+5	Dout
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	℃
Storage Temperature Range	T_{stg}	−65 to +125	℃
All Input and Output Voltages*	V_T	−0.3 to +7	V
V_{PP} Supply Voltage*	V_{PP}	−0.3 to +28	V

* With respect to Ground

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=5.25V/0.4V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.85V	—	—	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IL}$	—	21	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE}=\overline{CE}=V_{IL}$	—	62	100	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

Note : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

● AC CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address to Output Delay	t_{ACC}	$\overline{OE}=\overline{CE}=V_{IL}$	—	—	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}=V_{IL}$	—	—	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	—	—	120	ns
$\overline{OE}$ High to Output Float*	t_{DF}	$\overline{CE}=V_{IL}$	0	—	100	ns
Address to Output Hold	t_{OH}	$\overline{OE}=\overline{CE}=V_{IL}$	0	—	—	ns

* : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● CAPACITANCE (Ta=25°C, f=1MHz)

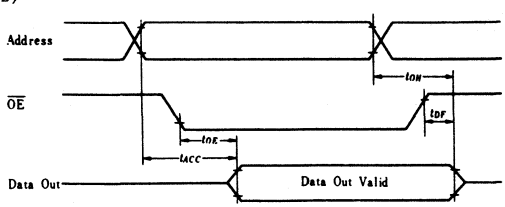
Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{IN}=0V	—	6	pF
Output Capacitance	C_{out}	V_{OUT}=0V	—	12	pF

● SWITCHING CHARACTERISTICS

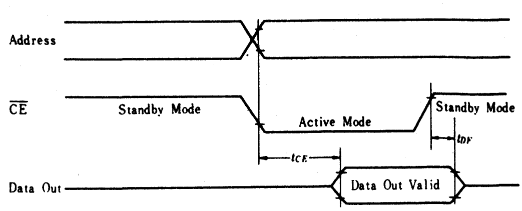
Test Conditions

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	≤ 20 ns
Output Load:	1TTL Gate + 100 pF
Reference Level for Measuring Timing:	Inputs 1V and 2V
	Outputs 0.8V and 2V

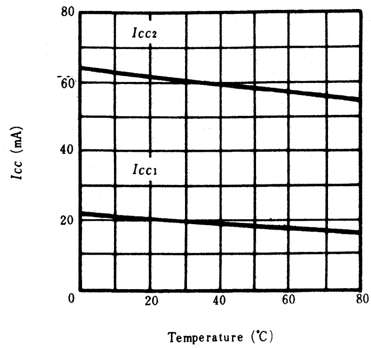
READ MODE ($\overline{CE}=V_{IL}$)

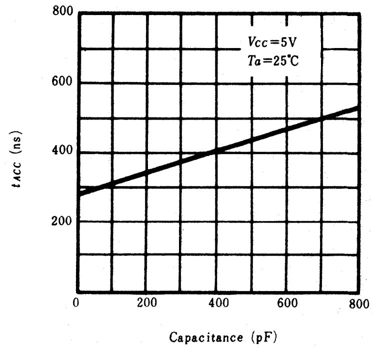


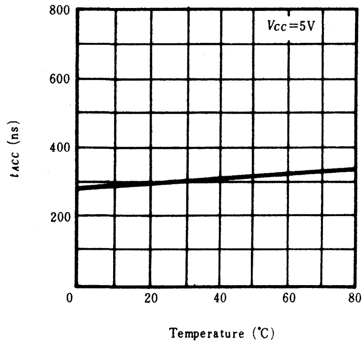
STANDBY MODE ($\overline{OE}=V_{IL}$)

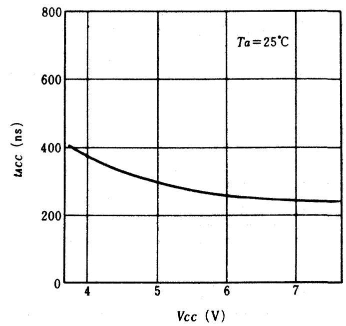


● TYPICAL CHARACTERISTICS









● DC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=25V±1V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
V_{PP} Supply Current	I_{PP1}	$\overline{CE}=V_{IL}$	—	—	6	mA
V_{PP} Supply Current During Programming	I_{PP2}	$\overline{CE}=V_{IH}$	—	—	30	mA
V_{CC} Supply Current	I_{CC}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	V_{CC}+1	V

● AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, V_{CC}=5V±5%, V_{PP}=25V±1V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		2	—	—	μs
$\overline{OE}$ Hold Time	t_{OEH}		5	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay*	t_{DF}	$\overline{CE}=V_{IL}$	0	—	120	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	—	—	120	ns
Program Pulse Width	t_{PW}		45	50	55	ms
Program Pulse Rise Time	t_{PRT}		5	—	—	ns
Program Pulse Fall Time	t_{PFT}		5	—	—	ns

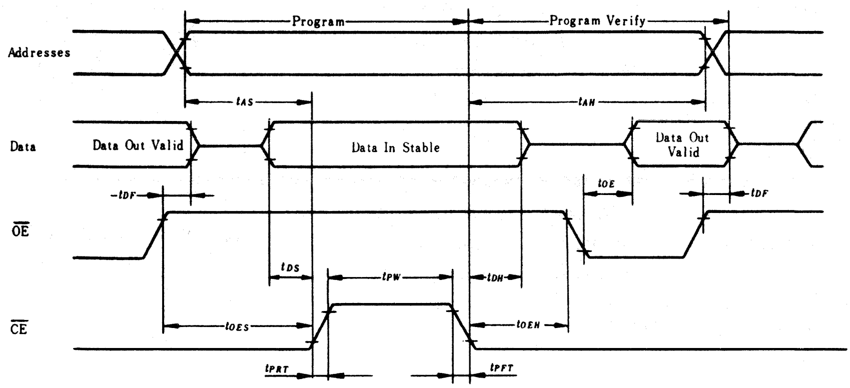
Notes : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
* : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Level: 0.8V to 2.2V
Input Rise and Fall Times: ≤ 20 ns
Output Load: 1 TTL Gate + 100 pF
Reference Level for Measuring Timing:
Inputs; 1V and 2V, Outputs; 0.8V and 2V

● PROGRAMMING WAVEFORMS



● ERASE

Erasure of HN462716 is performed by exposure to ultra-violet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure.
The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm²

■ DEVICE OPERATION

● READ MODE

Dataout is available 450ns (t_{ACC}) from addresses with $\overline{OE}$ low or 120ns (t_{OE}) from $\overline{OE}$ with addresses stable.

● DESELECT MODE

The outputs may be OR-tied together with the other HN462716s. When HN462716s are deselected, the $\overline{OE}$ inputs must be at high TTL level.

● POWER DOWN MODE

Power down is achieved with $\overline{CE}$ high TTL level. In this mode the outputs are in a high impedance state.

● PROGRAMMING

Initially, and after each erasure, all bits of the HN462716 are in the "High" state (Output High). Data is introduced by selectively programming "low" into the desired bit locations. In the programming mode, Vpp power supply is at 25V and $\overline{OE}$ input is at high TTL level. Data to be programmed are presented 8-bits in parallel, to the data output lines (O0 to O7).

The addresses and inputs are at TTL levels.
After the address and data setup, a 50 ms, active high program pulse is applied to the $\overline{CE}$ input. The $\overline{CE}$ is at TTL level.
The HN462716 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

● PROGRAM VERIFY

The HN462716 has a program verify mode. A verify should be performed on the programmed bits to determine that they were correctly programmed. In this mode Vpp is at 25V.

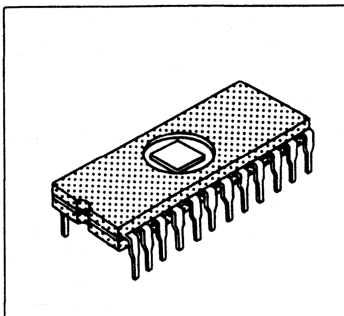
● PROGRAM INHIBIT

Programming of multiple HN462716s in parallel with different data is easily accomplished by using this mode. Except for $\overline{CE}$, all like inputs of the parallel HN462716s may be common.
A TTL program pulse applied to a HN462716's $\overline{CE}$ input will program that HN462716. A low level $\overline{CE}$ inhibits the other HN462716s from being programmed.

HN462716G-1, HN462716G-2

2048-word × 8-bit U. V. Erasable and Electrically Programmable Read Only Memory

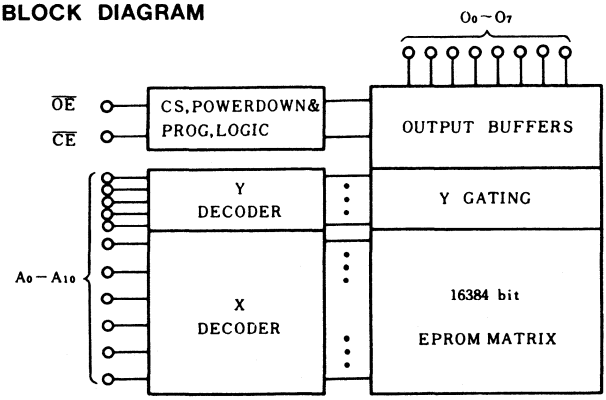
The HN462716 is a 2048 word by 8 bit erasable and electrically programmable ROMs. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to exposes the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.



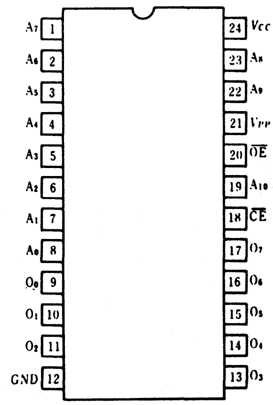
(DG-24B)

- Single Power Supply ······ +5V ±5%;
- Simple Programming ····· Program Voltage: +25V DC Programs with One 50ms Pulse
- Static ·················· No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded-on Chip Address Decode
- Access Time ············ 350ns Max.: HN462716G-1; 390ns Max.: HN462716G-2
- Low Power Dissipation ···· 555mW Max. Active Power; 161mW Max. Standby Power
- Three State Output ······· OR- Tie Capability
- Interchangeable with Intel 2716

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PROGRAMMING OPERATION

Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5	+5	Dout
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	Din
Program Verify	V_{IL}	V_{IL}	+25	+5	Dout
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
All Input and Output Voltages*	V_T	−0.3 to +7	V
V_{PP} Supply Voltage*	V_{PP}	−0.3 to +28	V

* With respect to Ground

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}= V_{CC}±0.6V)

Item	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT}=5.25V/0.4V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.85V	—	—	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IL}$	—	13	25	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE}=\overline{CE}=V_{IL}$	—	56	100	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

Note : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

● AC CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}= V_{CC}±0.6V)

Parameter	Symbol	Test Condition	HN462716G-1			HN462716G-2			Unit
			min	typ	max	min	typ	max	
Address to Output Delay	t_{ACC}	$\overline{OE}=\overline{CE}=V_{IL}$	—	—	350	—	—	390	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}=V_{IL}$	—	—	350	—	—	390	ns
$\overline{CE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	—	—	120	—	—	120	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}=V_{IL}$	0	—	100	0	—	100	ns
Address to Output Hold	t_{OH}	$\overline{OE}=\overline{CE}=V_{IL}$	0	—	—	0	—	—	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● CAPACITANCE (Ta=25°C, f=1MHz)

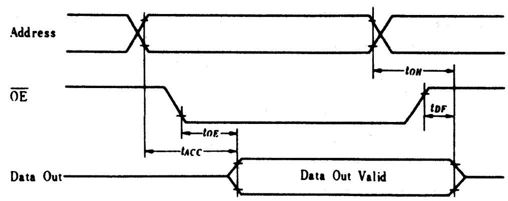
Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{IN}=0V	—	6	pF
Output Capacitance	C_{out}	V_{OUT}=0V	—	12	pF

● SWITCHING CHARACTERISTICS

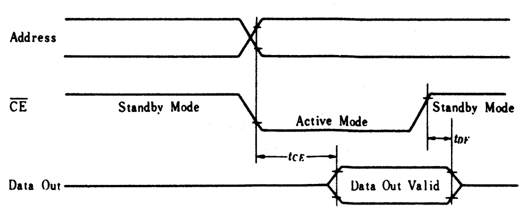
Test Conditions

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	≤ 20 ns
Output Load:	1TTL Gate + 100 pF
Reference Level for Measuring Timing:	Inputs 1V and 2V
	Outputs 0.8V and 2V

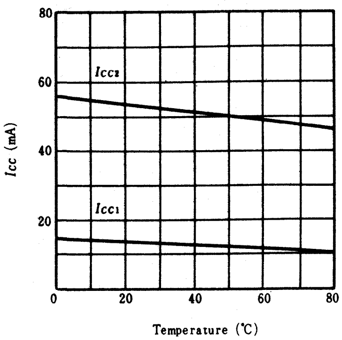
READ MODE ($\overline{CE}=V_{IL}$)

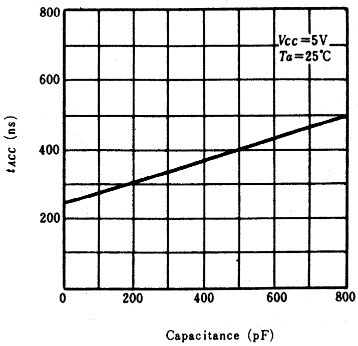


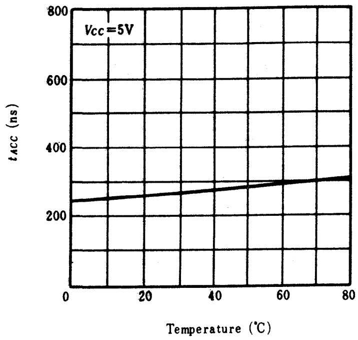
STANDBY MODE ($\overline{OE}=V_{IL}$)

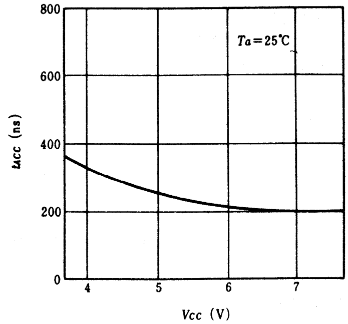


● TYPICAL CHARACTERISTICS









■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($Ta=25°C \pm 5°C$, $V_{CC}=5V \pm 5\%$, $V_{PP}=25V \pm 1V$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{CC}=5.25V$	—	—	10	μA
V_{PP} Supply Current	I_{PP1}	$\overline{CE}=V_{IL}$	—	—	5	mA
V_{PP} Supply Current During Programming	I_{PP2}	$\overline{CE}=V_{IH}$	—	—	30	mA
V_{CC} Supply Current	I_{CC}		—	—	100	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	$V_{CC}+1$	V

● AC PROGRAMMING CHARACTERISTICS ($Ta=25°C \pm 5°C$, $V_{CC}=5V \pm 5\%$, $V_{PP}=25V \pm 1V$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		2	—	—	μs
$\overline{OE}$ Hold Time	t_{OEH}		5	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}	$\overline{CE}=V_{IL}$	0	—	120	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	—	—	120	ns
Program Pulse Width	t_{PW}		45	50	55	ms
Program Pulse Rise Time	t_{PRT}		5	—	—	ns
Program Pulse Fall Time	t_{PFT}		5	—	—	ns

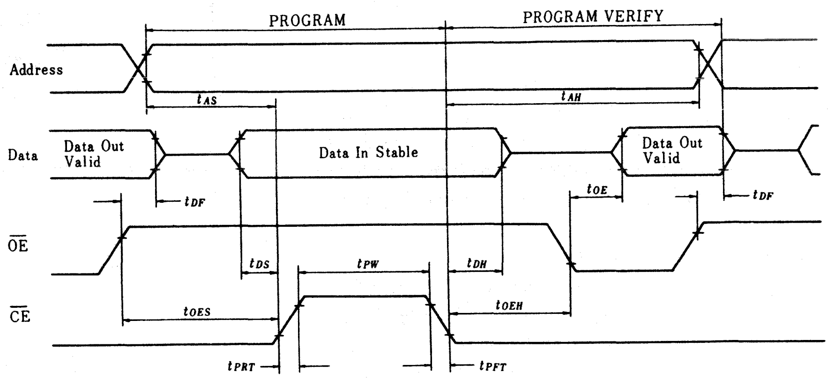
Note : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Times:	≤ 20 ns
Output Load:	1TTL Gate + 100 pF
Reference Level for Measuring Timing:	Inputs 1V and 2V
	Outputs 0.8V and 2V

● PROGRAMMING WAVEFORMS



● ERASE

Erasure of HN462716 is performed by exposure to ultra-violet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure.

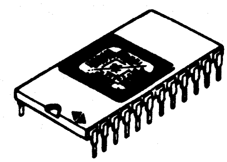
The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm^2.

HN462532, HN462532G, HN462532G-2

4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

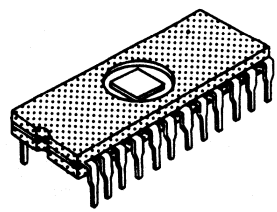
The HN462532 is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

HN462532



(DC-24C)

HN462532G,
HN462532G-2

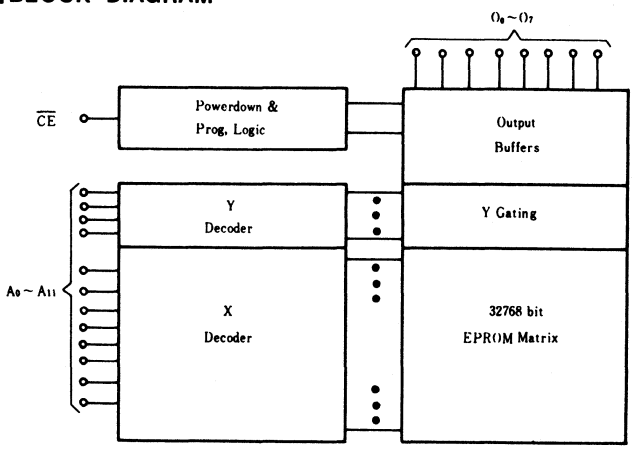


(DG-24B)

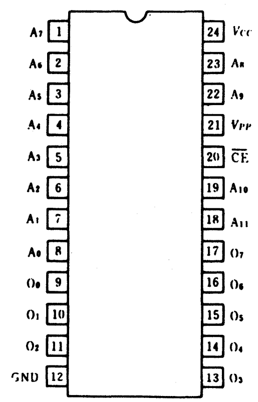
■ FEATURES

- Single Power Supply ...... +5V ±5%
- Simple Programming ..... Program Voltage: +25V D.C. Program with One 50ms Pulse
- Static .... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time .... 450ns (max.) HN462532/G 390ns (max.) HN462532G-2
- Low Power Dissipation .... 858mW (max) Active Power 201mW (max) Standby Power
- Three Stste Output .... OR-Tie Capability
- Compatible with TMS2532

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Pins / Mode	$\overline{CE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9 to 11, 13 to 17)
Read	V_{IL}	+5	+5	Dout
Stand by	V_{IH}	+5	+5	High Z
Program	Pulsed V_{IH} to V_{IL}	+25	+5	Din
Program Inhibit	V_{IH}	+25	+5	High Z

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltages*	V_T	−0.3 to +7	V
V_{PP} Voltage*	V_{PP}	−0.3 to +28	V
Operating Temperature Range	T_{opr}	0 to +70	℃
Storage Temperature Range	T_{stg}	−65 to +125	℃

* With respect to GND.

READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	−	−	10	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V/0.4V	−	−	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.85V	−	−	12	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}=V_{IH}$	−	−	25	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}=V_{IL}$	−	−	150	mA
Input Low Voltage	V_{IL}		−0.1	−	0.8	V
Input High Voltage	V_{IH}		2.0	−	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	−	−	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	−	−	V

Note : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

● AC CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

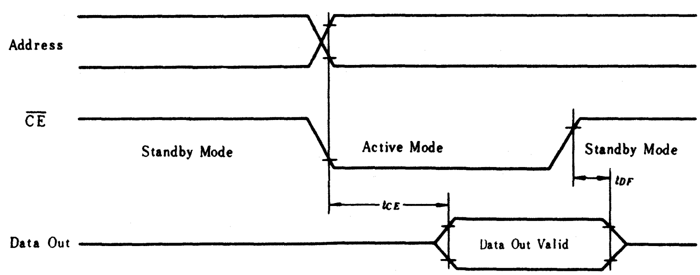
Parameter	Symbol	Test Condition	HN462532G-2			HN462532/G			Unit
			min	typ	max	min	typ	max	
Address to Output Delay	t_{ACC}	$\overline{CE}=V_{IL}$	−	−	390	−	−	450	ns
$\overline{CE}$ to Output Delay	t_{CE}		−	−	390	−	−	450	ns
$\overline{CE}$ High to Output Float*	t_{DF}		0	−	100	0	−	100	ns
Address to Output Hold	t_{OH}	$\overline{CE}=V_{IL}$	0	−	−	0	−	−	ns

* : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	< 20 ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V, Outputs; 0.8V and 2V



● CAPACITANCE (Ta=25℃, f=1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	−	−	6	pF
Output Capacitance	C_{out}	V_{out}=0V	−	−	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($Ta=25°C\pm5°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=25V\pm1V$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{in}=5.25V/0.4V$	—	—	10	μA
V_{PP} Supply Current During Programming	I_{PP2}	$\overline{CE}=V_{IL}$	—	—	30	mA
V_{CC} Supply Current	I_{CC}		—	—	150	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	$V_{CC}+1$	V

● AC PROGRAMMING CHARACTERISTICS ($Ta=25°C\pm5°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=25V\pm1V$)

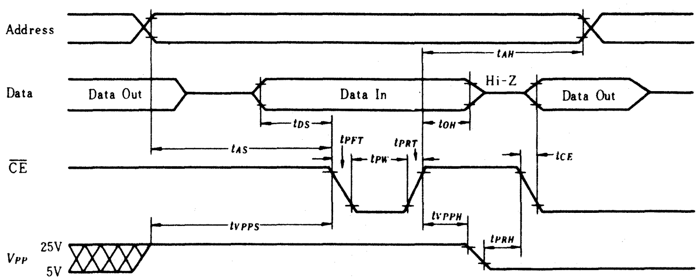
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		2	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
Setup Time from V_{PP}	t_{VPPS}		0	—	—	ns
Program Pulse Hold Time	t_{PRH}		0	—	—	ns
V_{PP} Hold Time	t_{VPPH}		0	—	—	ns
Program Pulse Width	t_{PW}		45	50	55	ms
Program Pulse Time	t_{PRT}		5	—	—	ns
Program Pulse Time	t_{PFT}		5	—	—	ns

Note : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

● SWITCHING CHARACTERISTICS

Test Conditions

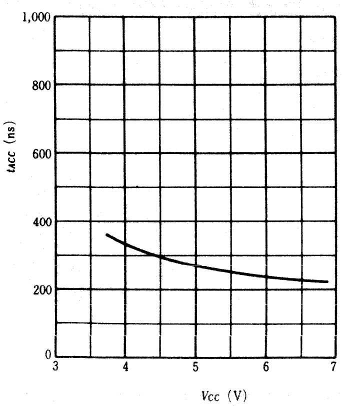
Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Times:	≤ 20 ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V, Outputs; 0.8V and 2V



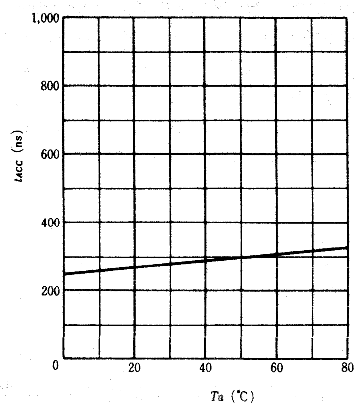
● ERASE

Erasure of HN462532 is performed by exposure to ultra-violet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure.
The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm².

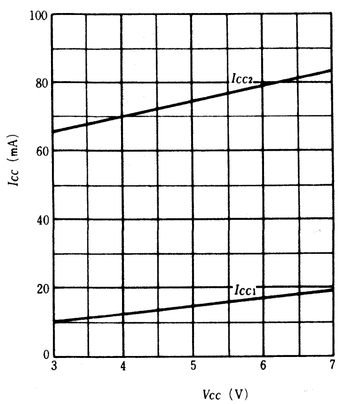
ACCESS TIME vs. SUPPLY VOLTAGE



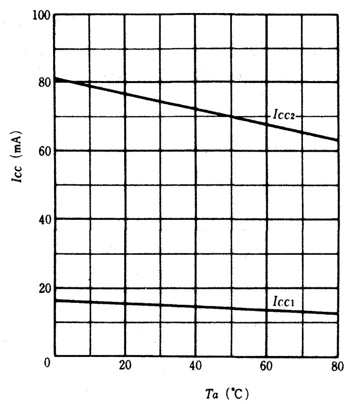
ACCESS TIME vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



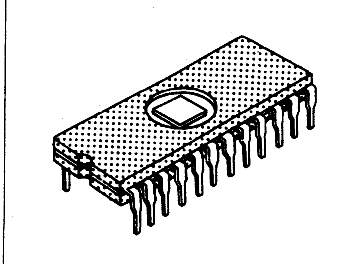
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



HN462532GL

4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The HN462532GL is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

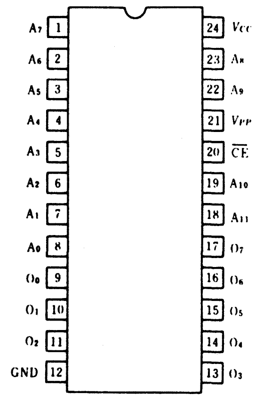


(DG-24B)

■ FEATURES

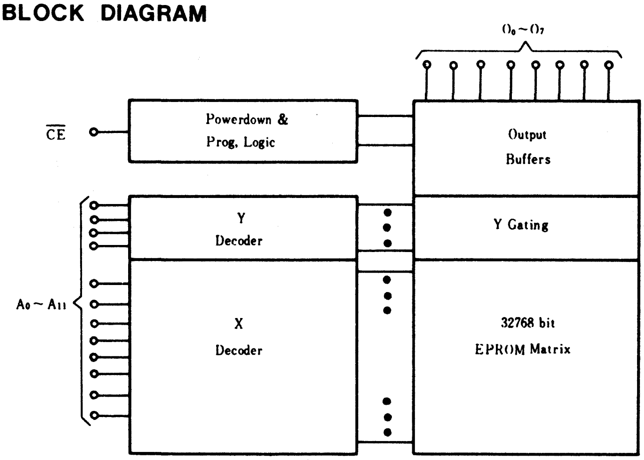
- Single Power Supply ...... +5V ±5%
- Simple Programming ...... Program Voltage: +25V D.C.
  Program with One 50ms Pulse
- Static .... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time .... 450ns (max)
- Low Power Dissipation .... 543mW (max) Active Power
  201mW (max) Standby Power
- Three State Output .... OR-Tie Capability
- Compatible with TMS25L32

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Pins / Mode	$\overline{CE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9 to 11, 13 to 17)
Read	V_{IL}	+5	+5	Dout
Stand-by	V_{IH}	+5	+5	High Z
Program	Pulsed V_{IH} to V_{IL}	+25	+5	Din
Program Inhibit	V_{IH}	+25	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltage	V_T	−0.3 to +7	V
V_{PP} Voltage*	V_{PP}	−0.3 to +28	V
Operating Temperature Range	T_{opr}	0 to +70	℃
Storage Temperature Range	T_{stg}	−65 to +125	℃

* With respect to GND.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	−	−	10	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V/0.4V	−	−	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.85V	−	−	12	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}=V_{IH}$	−	−	25	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}=V_{IL}$	−	−	95	mA
Input Low Voltage	V_{IL}		−0.1	−	0.8	V
Input High Voltage	V_{IH}		2.0	−	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	−	−	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	−	−	V

Note : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

● AC CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

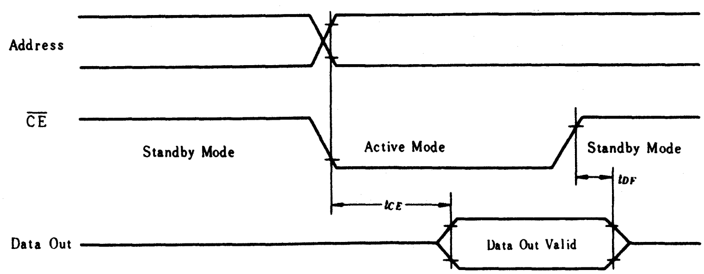
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address to Output Delay	t_{ACC}	$\overline{CE}=V_{IL}$	−	−	450	ns
$\overline{CE}$ to Output Delay	t_{CE}		−	−	450	ns
$\overline{CE}$ High to Output Float*	t_{DF}		0	−	100	ns
Address to Output Hold	t_{OH}	$\overline{CE}=V_{IL}$	0	−	−	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	< 20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V, Outputs; 0.8V and 2V



● CAPACITANCE (Ta=25℃, f=1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	−	−	6	pF
Output Capacitance	C_{out}	V_{out}=0V	−	−	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($Ta=25°C\pm5°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=25V\pm1V$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{in}=5.25V/0.4V$	—	—	10	μA
V_{PP} Supply Current During Programming	I_{PP2}	$\overline{CE}=V_{IL}$	—	—	30	mA
V_{CC} Supply Current	I_{CC}		—	—	95	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	$V_{CC}+1$	V

● AC PROGRAMMING CHARACTERISTICS ($Ta=25°C\pm5°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=25V\pm1V$)

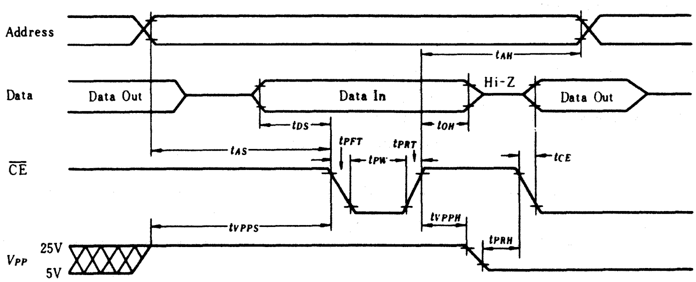
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		2	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
Setup Time from V_{PP}	t_{VPPS}		0	—	—	ns
Program Pulse Hold Time	t_{PRH}		0	—	—	ns
V_{PP} Hold Time	t_{VPPH}		0	—	—	ns
Program Pulse Width	t_{PW}		45	50	55	ms
Program Pulse Time	t_{PRT}		5	—	—	ns
Program Pulse Time	t_{PFT}		5	—	—	ns

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

● SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Times:	≤ 20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V, Outputs; 0.8V and 2V



● ERASE

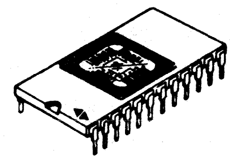
Erasure of HN462532 is performed by exposure to ultraviolet light with a wavelength of 2537Å, and all the output data are changed to "1" after this erasure procedure.
The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W · sec/cm².

HN462732, HN462732G, HN462732G-2

4096-word × 8-bit U.V. Erasable and Programmable Read Only Memory

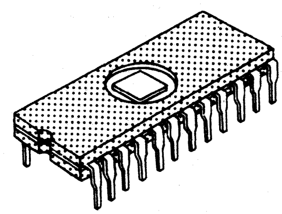
The HN462732 is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

HN462732



(DC-24C)

HN462732G
HN462732G-2

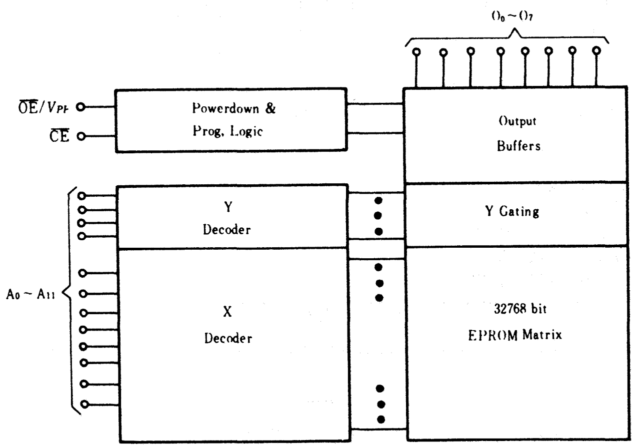


(DG-24B)

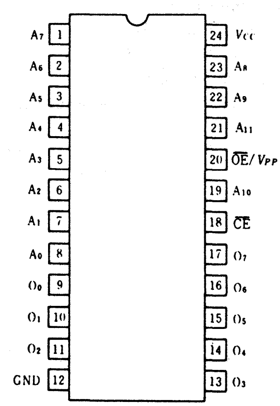
■ FEATURES

- Single Power Supply ...... +5V ±5%
- Simple Programming ...... Program Voltage: +25V D.C. Program with One 50ms Pulse
- Static .... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time .... 450ns (max) HN462732/G; 390ns (max) HN462732G-2
- Low Power Dissipation .... 150mA (max) Active Currents; 30mA (max) Standby Current
- Three State Output .... OR-Tie-Capability
- Compatible with INTEL 2732

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5	Dout
Stand by	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	Din
Program Verify	V_{IL}	V_{IL}	+5	Dout
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	℃
Storage Temperature Range	T_{stg}	−65 to +125	℃
All Input and Output Voltage*	V_T	−0.3 to +7	V
V_{PP} Voltage*	$\overline{OE}/V_{PP}$	−0.3 to +28	V

* With respect to GND

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current (Except $\overline{OE}/V_{PP}$)	I_{LI1}	V_{IN}=5.25V	−	−	10	μA
$\overline{OE}/V_{PP}$ Input Leakage Current	I_{LI2}	V_{IN}=5.25V	−	−	10	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V	−	−	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IL}$	−	−	30	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE}=\overline{CE}=V_{IL}$	−	−	150	mA
Input Low Voltage	V_{IL}		−0.1	−	0.8	V
Input High Voltage	V_{IH}		2.0	−	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	−	−	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	−	−	V

● AC CHARACTERISTICS (Ta=0 to +70℃, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

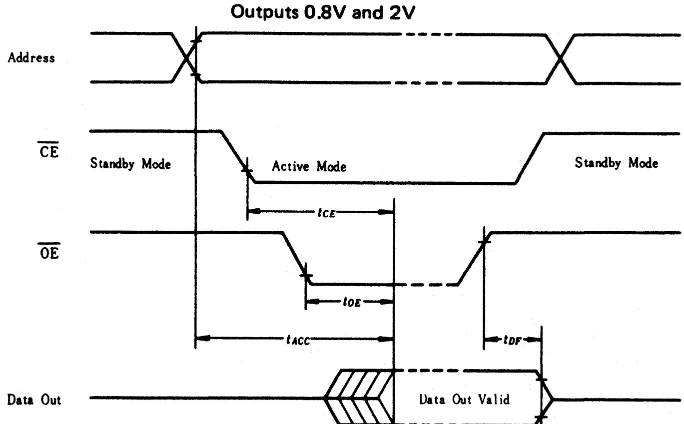
Parameter	Symbol	Test Condition	HN462732G-2			HN462732/G			Unit
			min.	typ.	max.	min.	typ.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	−	−	390	−	−	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}=V_{IL}$	−	−	390	−	−	450	ns
Output Enable to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	−	−	120	−	−	120	ns
Output Enable High to Output Float*	t_{DF}	$\overline{CE}=V_{IL}$	0	−	100	0	−	100	ns
Address to Output Hold	t_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	−	−	0	−	−	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	≦20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs 1V and 2V
	Outputs 0.8V and 2V



● CAPACITANCE (Ta=25℃, f=1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance (Except $\overline{OE}/V_{PP}$)	C_{IN1}	V_{IN}=0V	−	−	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}	V_{IN}=0V	−	−	20	pF
Output Capacitance	C_{out}	V_{out}=0V	−	−	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta=25°C±5°C)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V/0.4V	—	—	10	µA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400µA	2.4	—	—	V
V_{CC} Supply Current	I_{CC}		—	—	150	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level (All Input Except $\overline{OE}/V_{PP}$)	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{PP}$	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta=25°C±5°C)

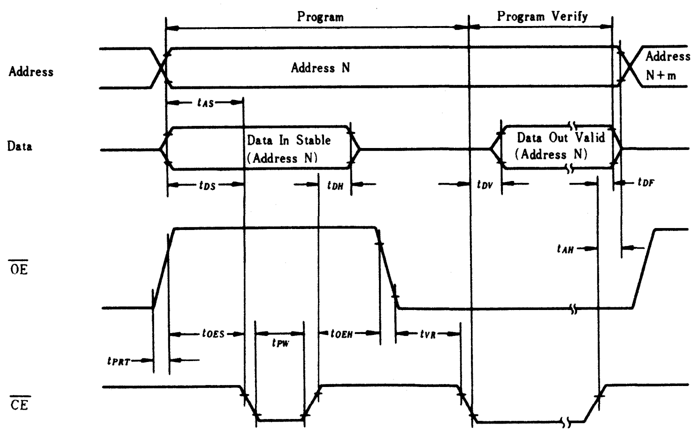
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	—	—	µs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	µs
Data Setup Time	t_{DS}		2	—	—	µs
Address Hold Time	t_{AH}		0	—	—	µs
$\overline{OE}$ Hold Time	t_{OEH}		2	—	—	µs
Data Hold Time	t_{DH}		2	—	—	µs
Chip Enable to Output Float Delay*	t_{DF}		0	—	120	ns
Data Valid from $\overline{CE}$	t_{DV}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IL}$	—	—	1	µs
$\overline{CE}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{OE}$ Pulse Rise Time During Programming	t_{PRT}		50	—	—	ns
V_{PP} Recovery Time	t_{VR}		2	—	—	µs

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Conditions

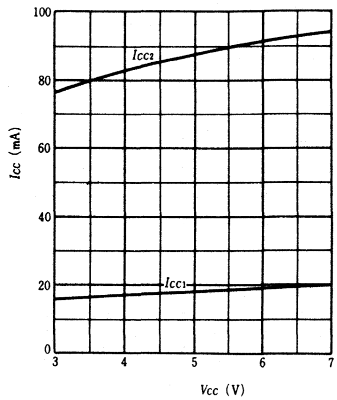
Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Times:	≤20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V, Outputs; 0.8V and 2V



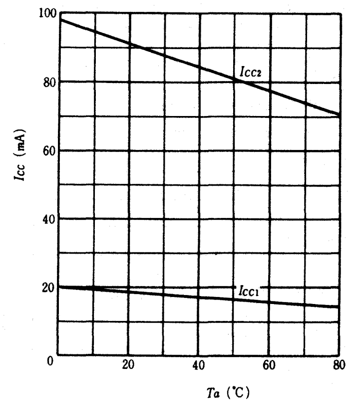
● ERASE

Erasure of HN462732 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this prosedure.
The minimum integrated close (i.e., UV intensity x exposure time) for erasure is 15W • sec/cm².

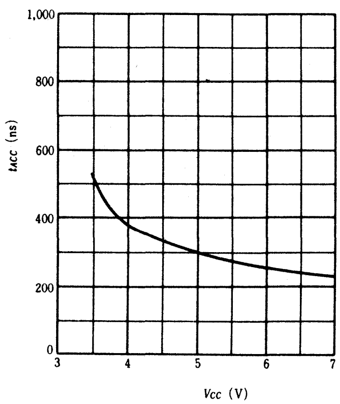
SUPPLY CURRENT vs. SUPPLY VOLTAGE



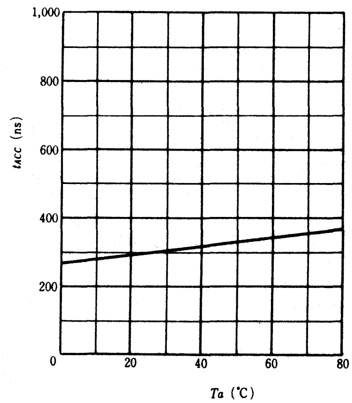
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ACCESS TIME vs. SUPPLY VOLTAGE



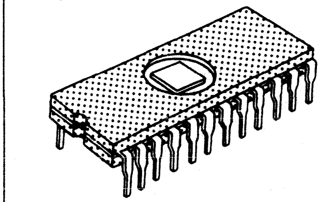
ACCESS TIME vs. AMBIENT TEMPERATURE



HN482732AG Series—Under Development —

4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The HN482732A is a 4096-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 24 pin dual-in-line package with transparent lid.
The transparent lid on the package allow the memory content to be erased with ultraviolet light.

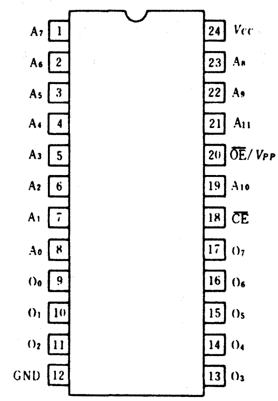


(DG-24B)

■ FEATURES

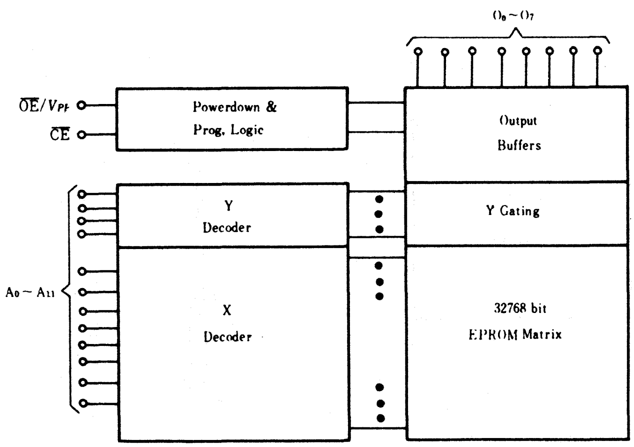
- Single Power Supply ...... +5V ±5%
- Simple Programming ...... Program Voltage: +21V D.C
  Program with one 50ms Pulse
- Static.................. No clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time .... HN482732AG-20 200ns (max)
  HN482732AG-25 250ns (max)
  HN482732AG-30 300ns (max)
- Absolute Max. Rating of Vpp Pin ... 28V
- Low Stand-by Current .... 35mA (max)
- Compatible with Intel 2732A

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM

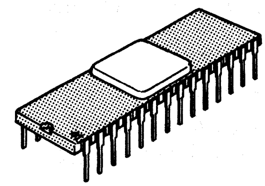


HN482764, HN482764-3
HN482764G, HN482764G-3 Preliminary

8192-word × 8-bit U. V. Erasable and Programmable Read Only Memory

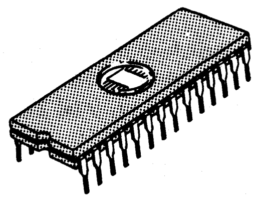
The HN482764 is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

HN482764, HN482764-3



(DC-28B)

HN482764G, HN482764G-3

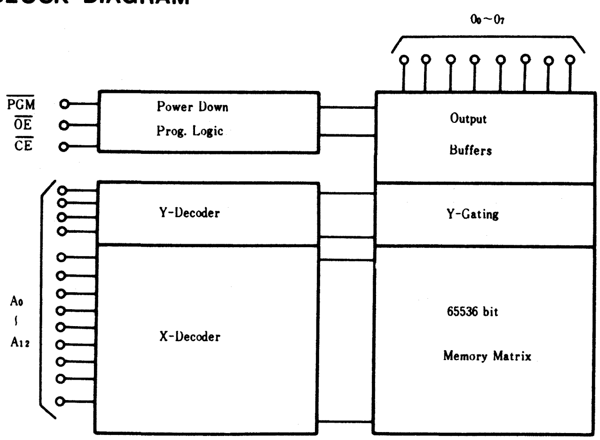


(DG-28)

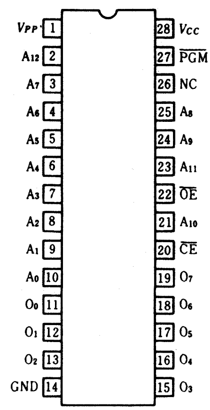
■ FEATURES

- Single Power Supply ...... +5V ± 5%
- Simple Programming ...... Program Voltage: +21V D.C.
  Program with one 50ms Pulse
- Static .... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time............. HN482764/G 250ns max
  HN482764/G-3 300ns max
- Absolute Max. Rating of Vpp pin ... 28V
- Low Stand-by Current............ 35mA max.
- Compatible with Intel 2764

■ BLOCK DIAGRAM



■ PIN ARRANGMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand-by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	℃
Storage Temperature Range	T_{stg}	−65 to +125	℃
All Input and Output Voltage*	V_T	−0.3 to +7	V
V_{PP} Voltage	V_{PP}	−0.3 to +28	V

* : with respect to GND

Note)
The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($Ta=0$ to $+70°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=V_{CC}\pm0.6V$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{CC}=5.25V$, $V_{in}=5.25V$	—	—	10	μA
Output Leakage Current	I_{LO}	$V_{CC}=5.25V$, $V_{out}=5.25V/0.4V$	—	—	10	μA
V_{PP} Current	I_{PP1}	$V_{PP}=V_{CC}+0.6V$	—	—	15	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}=V_{IH}$	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}=\overline{OE}=V_{IL}$	—	100	150	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	$V_{CC}+1$	V
Output Low Voltage	V_{OL}	$I_{OL}=2.1mA$	—	—	0.45	V
Output High Voltage	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	—	V

● AC CHARACTERISTICS ($Ta=0$ to $+70°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=V_{CC}\pm0.6V$)

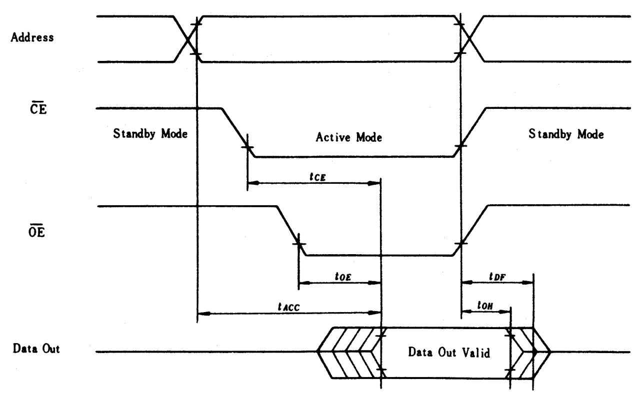
Parameter	Symbol	Test Condition	HN482764/G		HN482764/G-3		Unit
			min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	—	250	—	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}=V_{IL}$	—	250	—	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	10	100	10	150	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}=V_{IL}$	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	—	0	—	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≦ 20ns
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V Output; 0.8V and 2.0V



● CAPACITANCE ($Ta=25°C$, $f=1MHz$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	—	4	6	pF
Output Capacitance	C_{out}	$V_{out}=0V$	—	8	12	pF

PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($Ta=25°C\pm5°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=21V\pm0.5V$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{in}=5.25V$	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	$I_{OL}=2.1mA$	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	150	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	$V_{CC}+1$	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}=\overline{PGM}=V_{IL}$	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS ($Ta=25°C\pm5°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=21V\pm0.5V$)

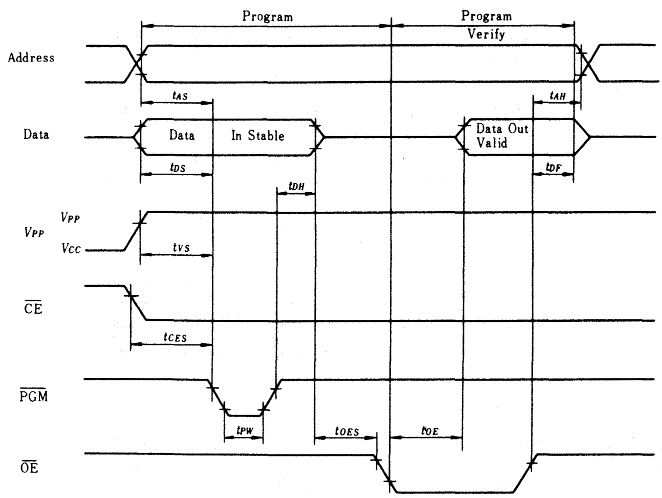
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20 ns
Reference Level for Measuring Timing:	Input; 1V and 2V Output; 0.8V and 2V



ERASE

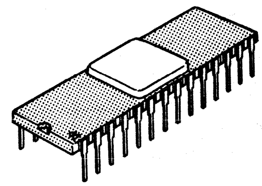
Erasure of HN482764 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W · sec/cm²

HN482764-4, HN482764G-4

8192-word × 8-bit U.V. Erasable and Programmable Read Only Memory

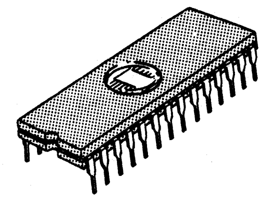
The HN482764 is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

HN482764-4



(DC-28B)

HN482764G-4

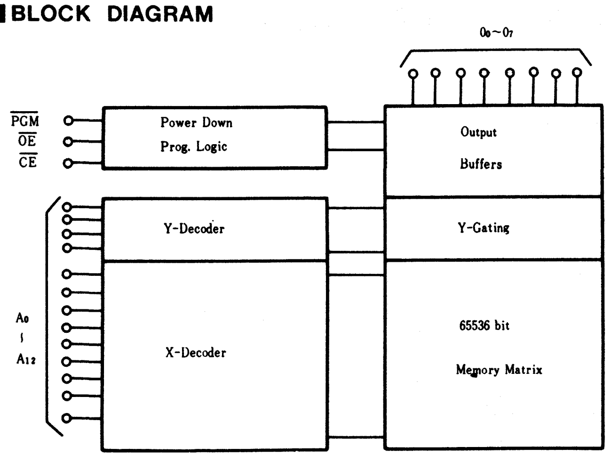


(DG-28)

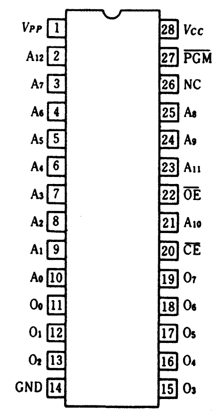
■ FEATURES

- Single Power Supply ..... +5V ±5%
- Simple Programming ...... Program Voltage: +21V D.C. Program with one 50ms Pulse
- Static .... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time............. 450ns max.
- Absolute Max. Rating of Vpp Pin ... 28V
- Low Stand-by Current........... 35mA max.
- Compatible with Intel 2764

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

× : Don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
All Input and Output Voltage*	V_T	−0.3 to +7	V
V_{PP} Voltage	V_{PP}	−0.3 to +28	V

* : With respect to GND

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{CC}=5.25V, V_{in}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{CC}=5.25V, V_{out}=5.25V/0.4V	—	—	10	μA
V_{PP} Current	I_{PP1}	V_{PP}=V_{CC}+0.6V	—	—	15	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$=V_{IH}	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	100	150	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

● AC CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

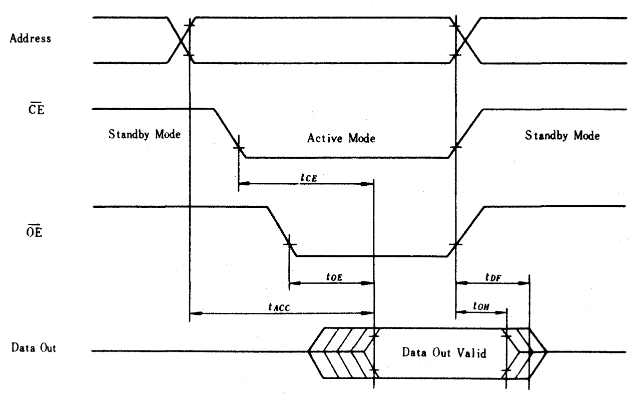
Parameter	Symbol	Test Condition	min.	max.	Unit
Address to Output Delay	t_{ACC}	$\overline{CE}$=$\overline{OE}$=V_{IL}	—	450	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$=V_{IL}	—	450	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$=V_{IL}	10	150	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$=V_{IL}	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	ns

Note : t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20ns
Output Load:	1TTL Gate +100pF
Reference Level for Measuring Timing:	Inputs; 1V and 2V Output; 0.8V and 2.0V



● CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	—	4	6	pF
Output Capacitance	C_{out}	V_{out}=0V	—	8	12	pF

PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($Ta=25\pm5$°C, $V_{CC}=5V\pm5\%$, $V_{PP}=21V\pm0.5V$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{in}=5.25V$	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	$I_{OL}=2.1mA$	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	150	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level	V_{IH}		2.0	—	$V_{CC}+1$	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}=\overline{PGM}=V_{IL}$	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS ($Ta=25$°C±5°C, $V_{CC}=5V\pm5\%$, $V_{PP}=21V\pm0.5V$)

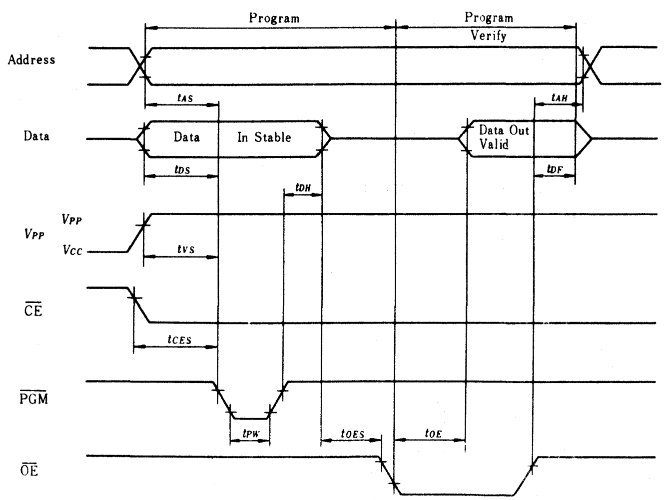
Parameter	Symbol	Test Condition	min	typ.	max.	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{OE}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
$\overline{PGM}$ Pulse width During Programming	t_{PW}		45	50	55	ms
$\overline{CE}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{OE}$	t_{OE}		—	—	150	ns

Note: t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20ns
Reference Level for Measuring Time:	Input; 1V and 2V
	Output; 0.8V and 2V

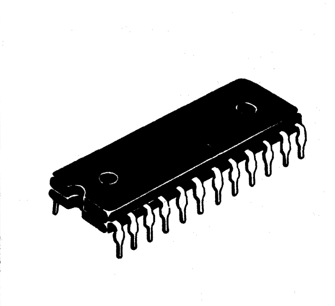


● ERASE

Erasure of HN482764 is performed by exposure to Ultraviolet light of 2537Å, and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W · sec/cm².

2048-word × 8-bit Electrically Erasable and Programmable ROM

This device operates from a single power supply and features fast single address location programming. All the words are erased by one TTL level pulse. Erasing the bit pattern and programming new pattern can be made within 42 seconds.

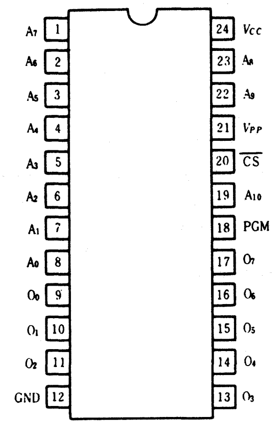


(DP-24)

■ FEATURES

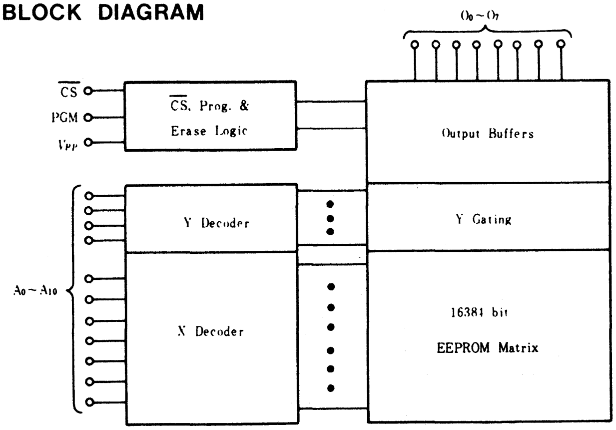
- Single Power Supply ...... +5V ±5%
- Simple Programming ...... Program voltage: +25V D.C. Program with one 20ms pulse.
- Electrically Erasing .... Erase Voltage: +25V D.C. Erase all words with one 200ms pulse.
- Fully Static .... No clocks required.
- Inputs and Outputs TTL compative during read, program and erase mode.
- Fully Decoded .... On-Chip Address Decode.
- Access Time .... 350ns Max.
- Low Power Dissipation .... 300mW Max.
- Three State Output .... OR-Tie Capability
- Pin-out Compatible with Intel 2716.

■ PIN. ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (8~11, 13~17)
Read	V_{IL}	V_{IL}	+5	+5	Dout
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	Din
Program Verify	V_{IL}	V_{IL}	+25	+5	Dout
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z
Erase	Pulsed V_{IL} to V_{IH}	V_{IL}	+25	+5	High Z

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
All Input and Output Voltage	V_{IN}, V_{out}	-0.3 to $V_{CC}+0.3$ or $V_{PP}+0.3$	V
V_{CC} Voltage	V_{CC}	-0.3 to $+7.0$	V
V_{PP} Voltage	V_{PP}	-0.3 to $+28$	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to $+125$	°C

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V\pm5\%$, $V_{PP}=V_{CC}\pm0.6V$,* $Ta=0$ to $+70$°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN}=5.25V$	–	–	10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=5.25V$	–	–	10	μA
V_{CC} Current	I_{CC1}	$\overline{CS}=V_{IH}/V_{IL}$	–	32	50	mA
V_{PP} Current	I_{PP1}	$V_{PP}=5.85V$	–	4	7	mA
Input Voltage	V_{IL}		-0.1	–	0.8	V
	V_{IH}		2.0	–	–	V
Output Voltage	V_{OL}	$I_{OL}=1.6mA$	–	–	0.4	V
	V_{OH}	$I_{OH}=-100\mu A$	2.4	–	–	V

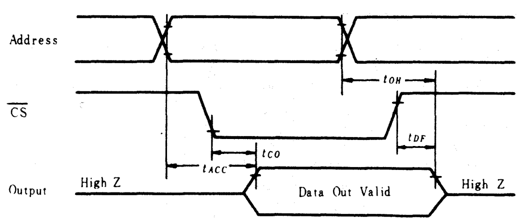
* The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.

● AC CHARACTERISTICS ($V_{CC}=5V\pm5\%$, $V_{PP}=V_{CC}\pm0.6V$, $Ta=0$ to $+70$°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address to Output Delay	t_{ACC}	PGM $=\overline{CS}=V_{IL}$	–	200	350	ns
Chip Select to Output Delay	t_{CO}	PGM $=V_{IL}$	–	70	150	ns
Chip Deselect to Output Float	t_{DF}		0	40	100	ns
Address to Output Hold	t_{OH}	PGM $=\overline{CS}=V_{IL}$	10	–	–	ns

● TEST CONDITION

Input pulse levels: 0.8V to 2.0V
Input rise and fall time: ≦ 20ns
Output load: 1TTL Gate + 100 pF
Reference level for Measuring Timing: Inputs 1V and 1.8V
Outputs 0.8V and 2.0V



● CAPACITANCE ($Ta=25$°C, $f=1MHz$)

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0V$	–	7.5	pF
Output Capacitance	C_{out}	$V_{out}=0V$	–	15	pF

PROGRAM OPERATION

● DC PROGRAMMING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta=0 to +70℃)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
V_{CC} Supply Current	I_{CC2}		—	32	50	mA
V_{PP} Supply Current	I_{PP2}		—	10	20	mA
Input Voltage	V_{IL}		−0.1	—	0.8	V
	V_{IH}		2.0	—	—	V

● AC PROGRAMMING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta=0 to +70℃)

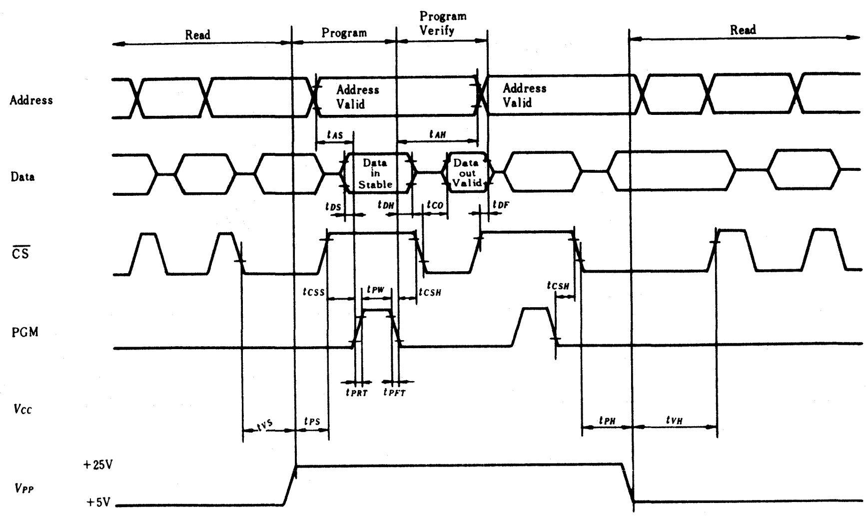
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{CS}$ Setup Time	t_{CSS}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		2*	—	—	μs
$\overline{CS}$ Hold Time	t_{CSH}		7	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
Chip Deselect to Output Float Delay	t_{DF}		0	40	100	ns
Chip Select to Output Delay	t_{CO}		—	70	150	ns
Program Pulse Width	t_{PW}		15	20	25	ms
Program Pulse Rise Time	t_{PRT}		5	—	—	ns
Program Pulse Fall Time	t_{PFT}		5	—	—	ns
V_{PP} Setup Time	t_{PS}		10	—	—	μs
V_{PP} Hold Time	t_{PH}		10	—	—	μs
$\overline{CS}$ to Program Mode Time	t_{VS}		10	—	—	μs
V_{PP} Read Mode Time	t_{VH}		10	—	—	μs

* If the mode changes from program mode to program verify mode sequentially (in the same address), t_{AH} must be larger than t_{CSH} + t_{CO}.

● TEST CONDITION

Test Condition

Input pulse levels:	0.8V to 2.0V
Input rise and fall time:	20ns (10% to 90%)
Reference level for Measuring Timing:	Input; 1V and 1.8V
	Output: 0.8V and 2.0V



■ ERASE OPERATION

● DC ERASING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta= 0 to +70℃)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
V_{CC} Supply Current	I_{CC3}		—	32	50	mA
V_{PP} Supply Current	I_{PP3}		—	10	20	mA
Input Voltage	V_{IL}		−0.1	—	0.8	V
	V_{IH}		2.0	—	—	V

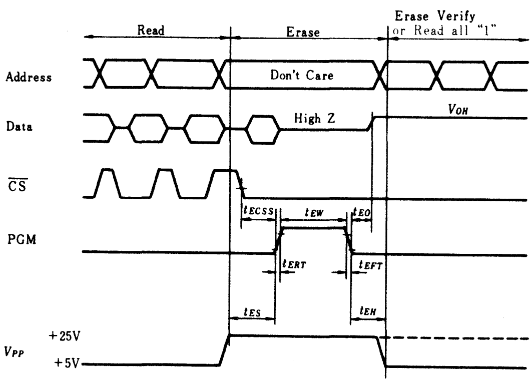
● AC ERASING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta= 0 to +70℃)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
$\overline{CS}$ Setup Time	t_{ECSS}		2	—	—	μs
PGM to Output Delay	t_{EO}		2	—	—	μs
Erase Pulse Width	t_{EW}		190	200	210	ms
Erase Pulse Rise Time	t_{ERT}		5	—	—	ns
Erase Pulse Fall Time	t_{EFT}		5	—	—	ns
V_{PP} Setup Time	t_{ES}		10	—	—	μs
V_{PP} Hold Time	t_{EH}		10	—	—	μs
Erase Program Time t_{EP}	t_{EP}		10	—	—	μs
Program Enase Time t_{PE}	t_{PE}		10	—	—	μs

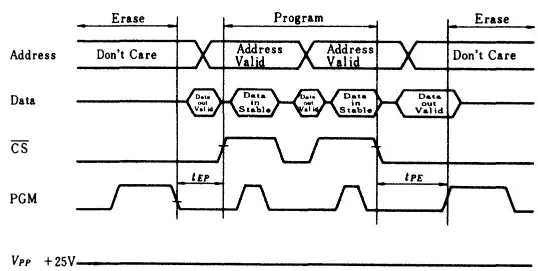
● TEST CONDITION

Test Condition

Input pulse levels:	0.8V to 2.0V
Input rise and fall time:	20ns (10% to 90%)
Reference level for Measuring Timing:	Input; 1V and 1.8V
	Output; 0.8V and 2.0V



● Erasing→Programming→Erasing



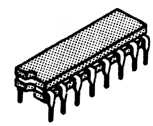
BIPOLAR RAM

HM2105

256-word × 1-bit Fully Decoded Random Access Memory

The HM2105 is a 256-word x 1-bit read/write random access memory developed for application to buffer memory, control memory, etc.

- Level .... 10K ECL compatible
- Chip select access time .... 12ns (max)
- Address access Time .... 35ns (max)
- Power Consumption .... 1.8mW/bit (typ)
- Output obtainable by Wired-OR (open emitter)



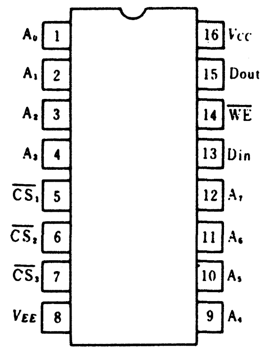
(DG-16)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout*	Read

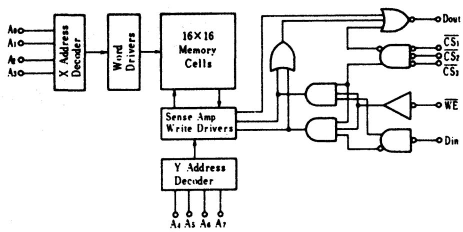
× : Don't care
* : Read out non-inverted

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	− 980	—	—	
			+75°C	− 920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other $V_{IN}=V_{ILB}$		−50	—	—	
Power Supply Current	I_{EE}	All Input and Output Open. Test pin 8.	+75°C	−120	−85	—	mA
			0°C	−130	−95	—	

● AC CHARACTERISTICS

($V_{EE}=-5.2V\pm5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	7	12	ns
Chip Select Recovery Time	t_{RCS}		—	7	12	ns
Address Access Time	t_{AA}		—	20	35	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=8ns$	25	15	—	ns
Data Setup Time	t_{WSD}		5	3	—	ns
Data Hold Time	t_{WHD}		5	3	—	ns
Address Setup Time	t_{WSA}	$t_W=25ns$	8	5	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		5	3	—	ns
Chip Select Hold Time	t_{WHCS}		5	3	—	ns
Write Disable Time	t_{WS}		3	14	—	ns
Write Recovery Time	t_{WR}		—	15	20	ns

3. RISE AND FALL TIME

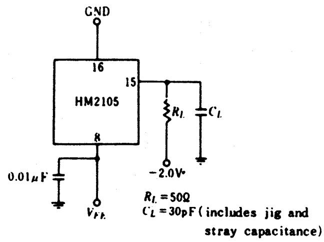
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		—	5	—	ns
Output Fall Time	t_f		—	5	—	ns

4. CAPACITANCE

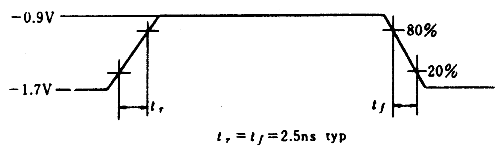
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Lead Capacitance	C_{in}		—	4	5	pF
Output Lead Capacitance	C_{out}		—	7	8	pF

■ TEST CIRCUIT AND WAVEFORMS

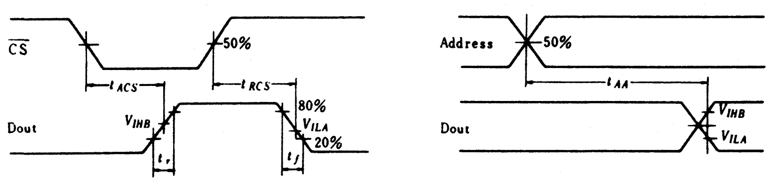
1. LOADING CONDITION



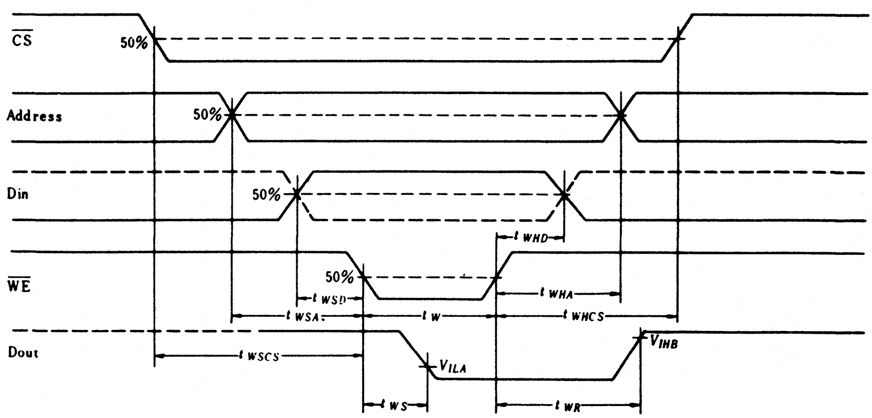
2. INPUT PULSE



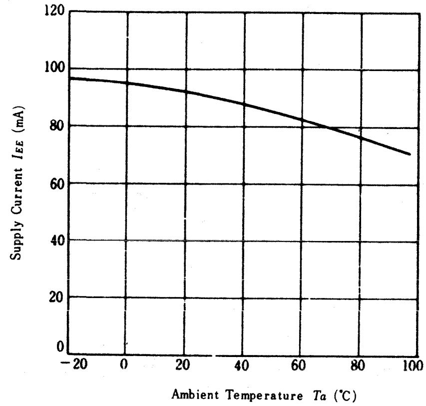
3. READ MODE



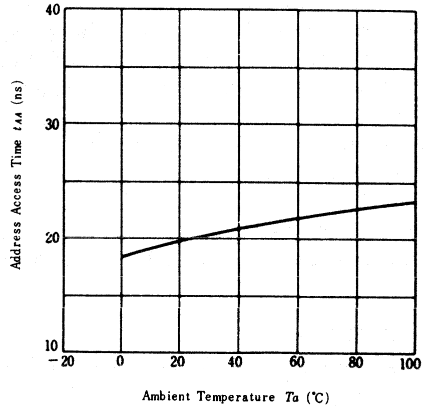
4. WRITE MODE



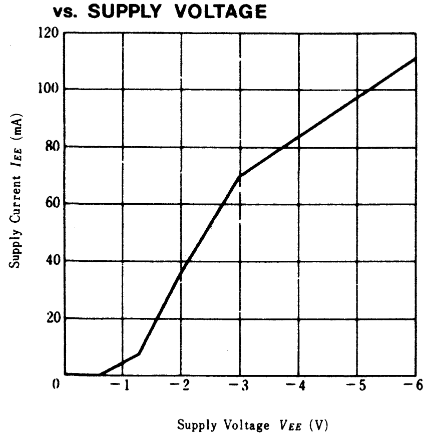
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

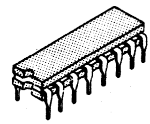


HM2106

256-word × 1-bit Fully Decoded Random Access Memory

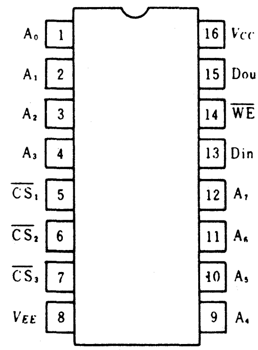
The HM2106 is an ECL compatible, 256-word x 1-bit, read/write random access memory developed for application to scratch pad, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time .... 10ns (max)
- Address Access time .... 15ns (max)
- Power consumption .... 1.8mW/bit (typ)
- Output obtainable by wired-OR (open emitter)



(DG-16)

■ PIN ARRANGEMENT



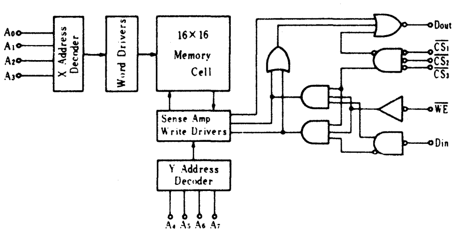
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout *	Read

× : Don't care
* : Read out non-inverted

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2106	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperarature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg}(Bias)*	−55 to +125	℃

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition			min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}		0°C	−1000	—	−840	mV
				+25°C	−960	—	−810	
				+75°C	−900	—	−720	
	V_{OL}			0°C	−1870	—	−1665	
				+25°C	−1850	—	−1650	
				+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}		0°C	−1020	—	—	mV
				+25°C	−980	—	—	
				+75°C	−920	—	—	
	V_{OLC}			0°C	—	—	−1645	
				+25°C	—	—	−1630	
				+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Input		0°C	−1145	—	−840	mV
				+25°C	−1105	—	−810	
				+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs		0°C	−1870	—	−1490	
				+25°C	−1850	—	−1475	
				+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$		0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	$V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other			−50	—	—	
Supply Current	I_{EE}	All Input and Output Open. Test pin 8.		+75°C	−120	−85	—	mA
				0°C	−130	−95	—	

●AC CHARACTERISTICS

($V_{EE}=-5.2V\pm5\%$, $Ta=0$ to $+75^\circ C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	6	10	ns
Chip Select Recovery Time	t_{RCS}		—	6	10	ns
Address Access Time	t_{AA}		3	9	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=2$ns	10	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	$t_W=10$ns	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		3	—	—	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

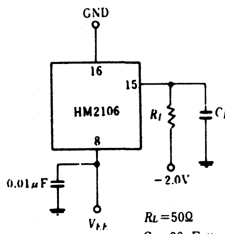
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Output Rise Time	t_r		—	3	—	ns
Output Fall Time	t_f		—	3	—	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}		—	2	5	pF
Output Capacitance	C_{out}		—	3	8	pF

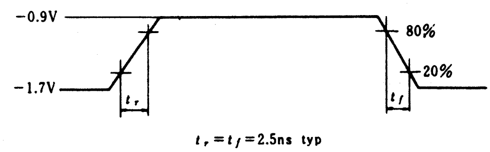
■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

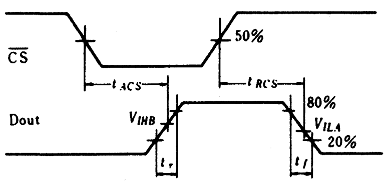


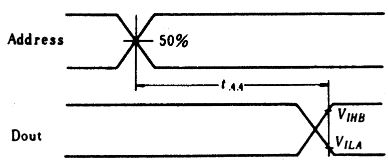
R_L=50Ω
C_L=30pF (includes jig and stray capacitance)

2. INPUT PULSE

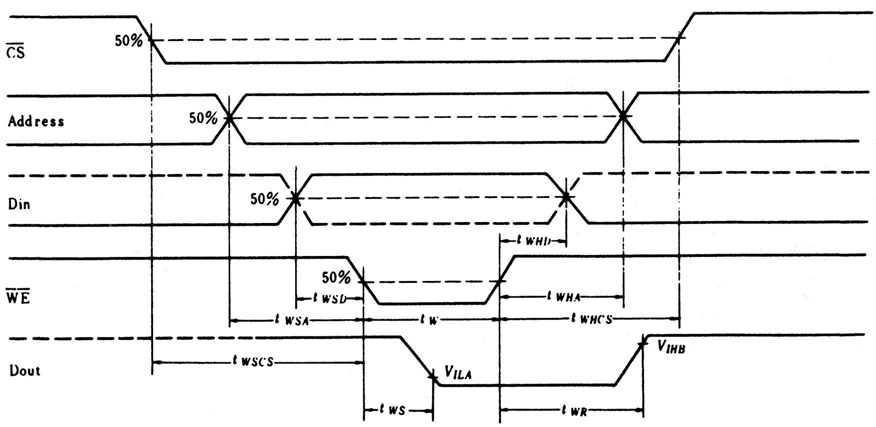


3. READ MODE

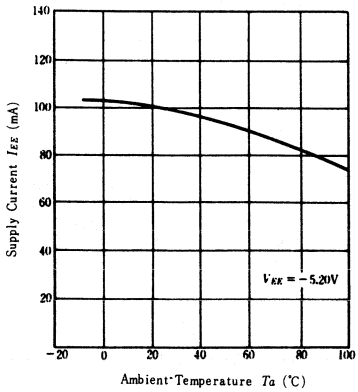




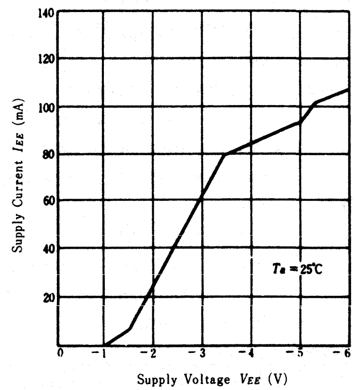
4. WRITE MODE



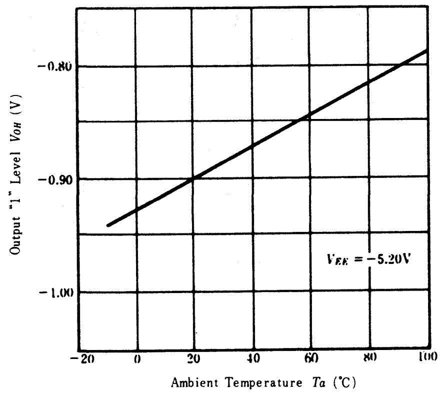
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



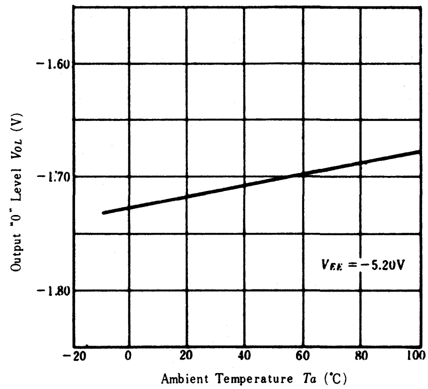
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



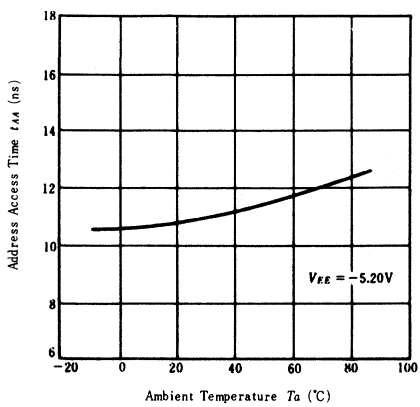
OUTPUT "1" LEVEL
vs. AMBIENT TEMPERATURE



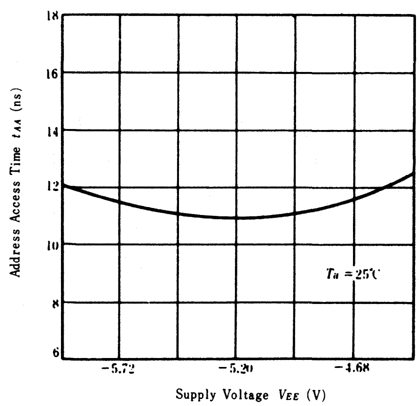
OUTPUT "0" LEVEL
vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME
vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME
vs. SUPPLY VOLTAGE

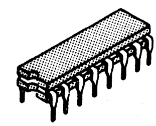


HM10414, HM10414-1

256-word × 1-bit Fully Decoded Random Access Memory

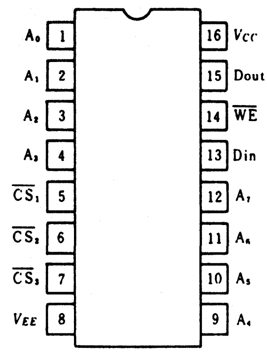
The HM10414 is ECL 10K compatible, 256-word x 1-bit, read write, random access memory developed for high speed systems such as scratch pad and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10414 is encapsulated in cerdip-16pin package, compatible with Fairchild's F10414.

- Fully compatible with 10K ECL level
- Address access time: HM10414: 10ns (max.)
  HM10414-1: 8ns (max.)
- Write pulse width: 6ns (min.)
- Three chip select pins
- Output obtainable by wired-OR (open emitter)



(DG-16)

■ PIN ARRANGEMENT



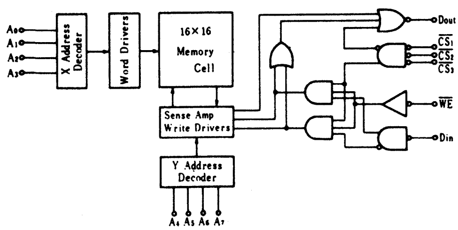
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout*	Read

× : Don't care
* : Read out non-inverted

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ ($V_{IN}=V_{ILB}$)	0 to +75°C	0.5	—	170	
		Other ($V_{IN}=V_{ILB}$)		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	+75°C	—	−130	—	mA
			0°C	−180	−140	—	

● AC CHARACTERISTICS

($V_{EE}=-5.2V\pm5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM10414 min	HM10414 typ	HM10414 max	HM10414-1 min	HM10414-1 typ	HM10414-1 max	Unit
Chip Select Access Time	t_{ACR}		—	3	6	—	3	6	ns
Chip Select Recovery Time	t_{RCS}		—	3	6	—	3	6	ns
Address Access Time	t_{AA}		—	7	10	—	6	8	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=2$ns	6	4	—	ns
Data Setup Time	t_{WSD}		1	0	—	ns
Data Hold Time	t_{WHD}		1	0	—	ns
Address Setup Time	t_{WSA}	$t_W=6$ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		1	0	—	ns
Chip Select Hold Time	t_{WHCS}		1	0	—	ns
Write Disable Time	t_{WS}		—	—	5	ns
Write Recovery Time	t_{WR}		—	—	5	ns

3. RISE/FALL TIME

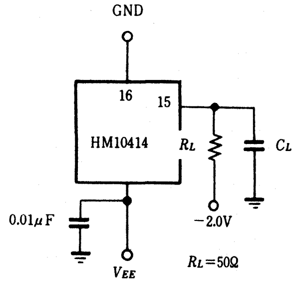
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	1.5	2.5	ns
Output Fall Time	t_f		—	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	5	pF
Output Capacitance	C_{out}		—	5	8	pF

■ TEST CIRCUIT AND WAVEFORMS

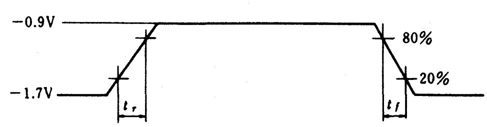
1. LOADING CONDITIONS



R_L=50Ω

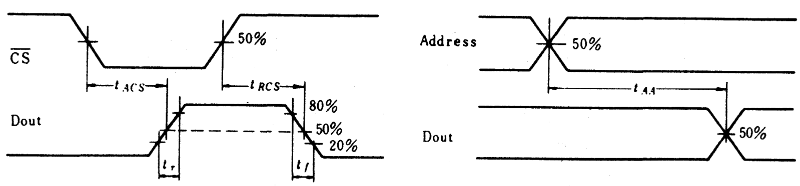
C_L=30pF(includes jig and stray capacitance)

2. INPUT PULSE

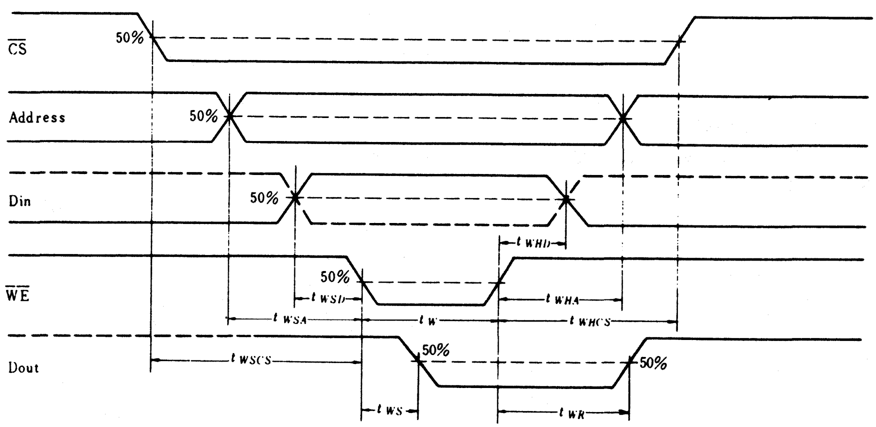


$t_r = t_f$ = 2.0ns typ

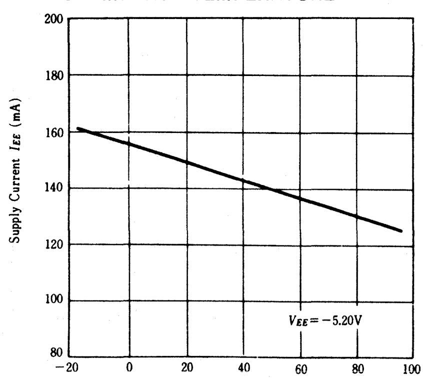
3. READ MODE



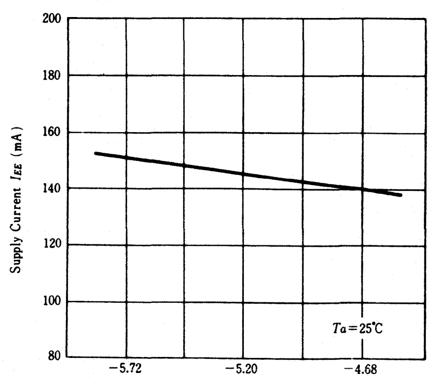
4. WRITE MODE



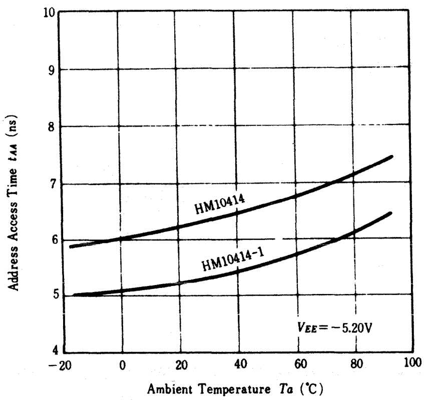
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



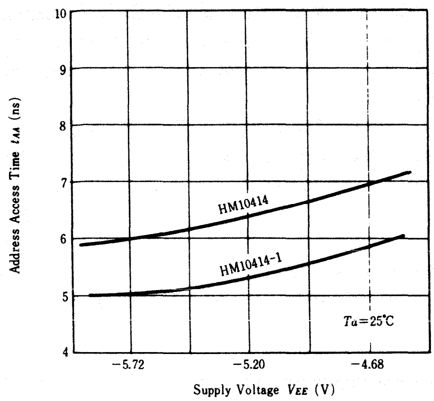
SUPPLY CURRENT vs. SUPPLY VOLTAGE



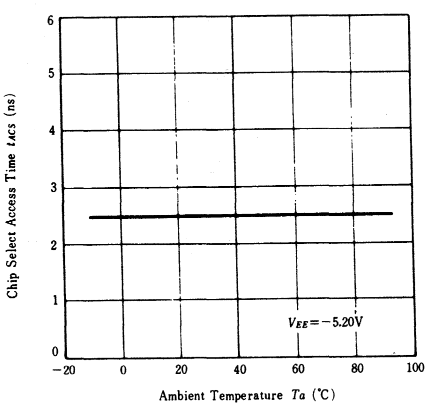
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



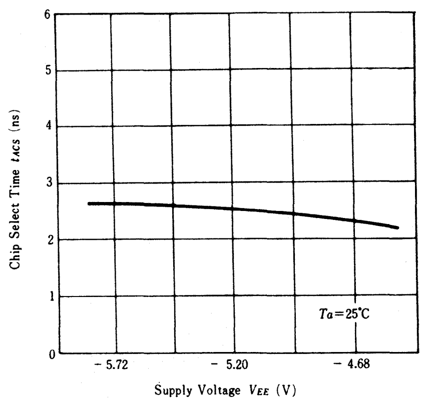
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



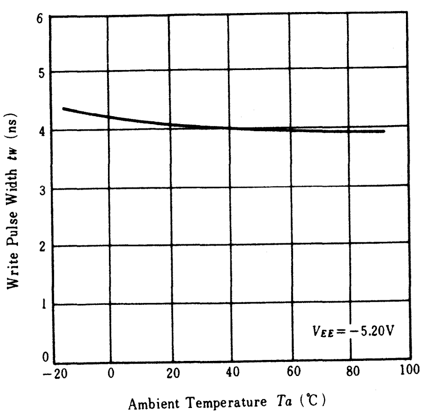
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



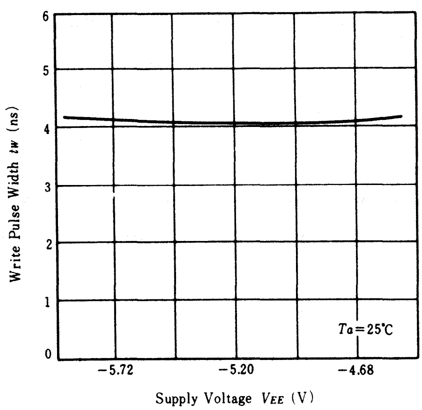
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

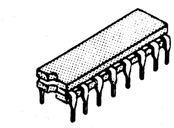


HM2110, HM2110-1, HM2110-2

1024-word × 1-bit Fully Decoded Random Access Memory

The HM2110 Series item is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time ....10ns (max.)
- Address access time .... HM2110: 35ns (max.)
  HM2110-1: 25ns (max.)
  HM2110-2: 20ns (max.)
- Power consumption ,................0.5mW/bit (typ)
- Output obtainable by Wired-OR (open emitter).



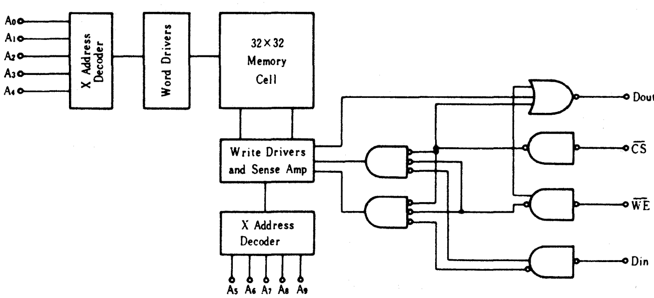
(DG-16A)

■ TRUTH TABLE

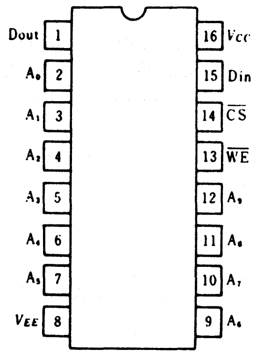
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

× : irrelevant
* : Read out noninverted

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXMUM RATINGS

Item	Symbol	HM2110 Series	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ — $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other — $V_{IN}=V_{ILB}$		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	$0\leqq Ta<25°C$	−150	−100	—	mA
			$Ta\geqq 25°C$	−125	−90	—	

● AC CHARACTERISTICS

($V_{EE}=-5.2V\ \pm5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			HM2110-2			Unit
			min	typ	max	min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	7	10	—	7	10	—	7	10	ns
Chip Select Recovery Time	t_{RCS}		—	7	10	—	7	10	—	7	10	ns
Address Access Time	t_{AA}		—	20	35	—	15	25	—	15	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			HM2110-2			Unit
			min	typ	max	min	typ	max	min	typ	max	
Write Pulse Width	t_W	$t_{WSA}=8ns$	25	—	—	25	—	—	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	5	—	—	5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	5	—	—	5	—	—	ns
Address Setup Time	t_{WSA}	$t_W=25ns$	8	—	—	8	—	—	8	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	5	—	—	5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	—	5	—	—	5	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	10	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	10	—	—	10	ns

3. RISE/FALL TIME

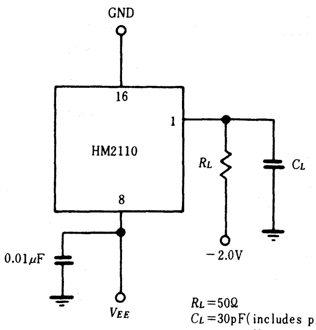
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	5	—	ns
Output Fall Time	t_f		—	5	—	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	5	pF
Output Capacitance	C_{out}		—	7	8	pF

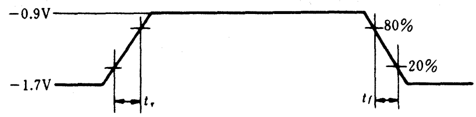
■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



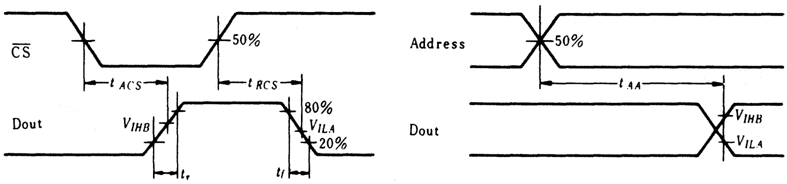
R_L = 50Ω
C_L = 30pF (includes probe and jig capacitance)

2. INPUT PULSE

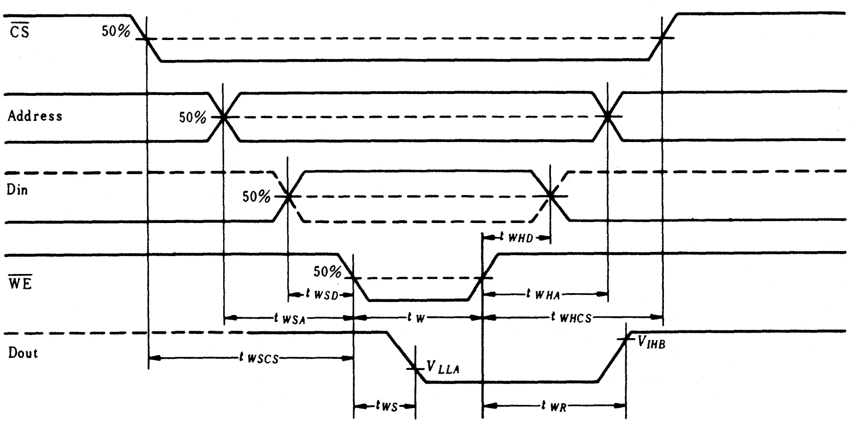


$t_r = t_f$ = 2.5ns typ

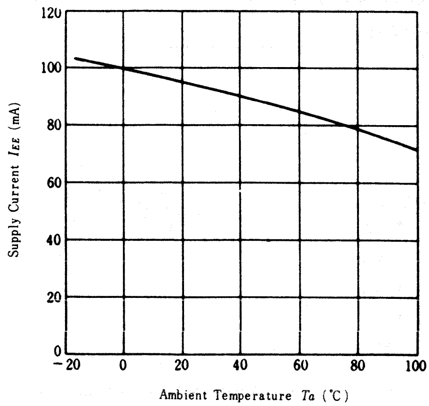
3. READ MODE



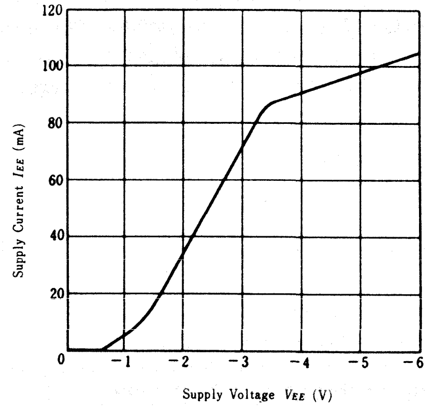
4. WRITE MODE



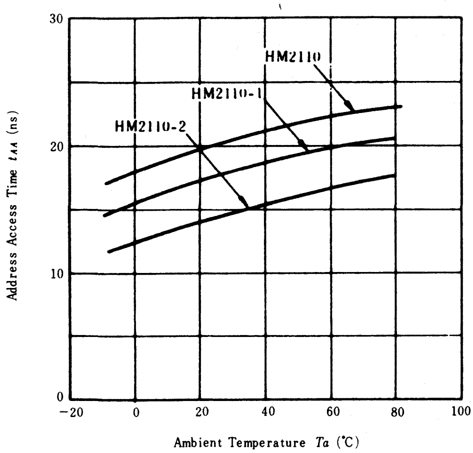
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



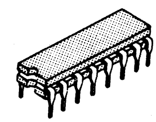
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HM2112, HM2112-1

1024-word×1-bit Fully Decoded Random Access Memory

The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

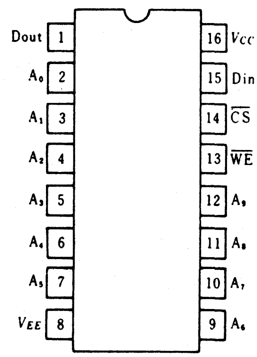


(DG-16A)

■ FEATURES

- Level .... 10k ECL Compatible
- Construction .... 1024-word by 1-bit
- Address Access Time .... HM2112 10ns (max.)
  HM2112-1 8ns (max.)
- Chip Select Access Time .... 5ns (max.)
- Power Consumption .... 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Fully Pin Compatible with F10415

■ PIN ARRANGEMENT



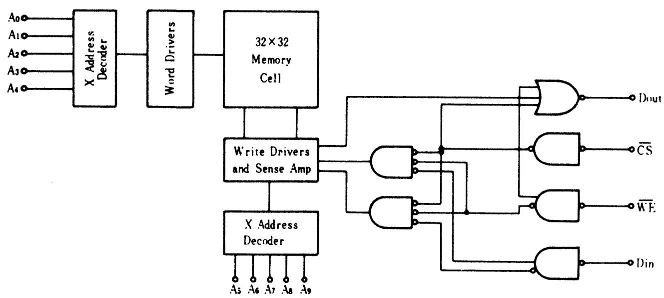
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

× : Irrelevant
* : Read out noniverted

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2112	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

($V_{EE}=-5.2$V, $R_L=50\Omega$ to -2.0V, $Ta=0$ to $+75$°C, air flow exceeding 2m/sec)

●DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IL}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ ($V_{IN}=V_{ILB}$)	0 to +75°C	0.5	—	170	
		Other ($V_{IN}=V_{ILB}$)		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	$Ta=0$°C	−200	—	—	mA
			$Ta=75$°C	−170	—	—	

●AC CHARACTERISTICS

($V_{EE}=-5.2$V ±5%, $Ta=0$ to $+75$°C, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		1	3	5	1	3	5	ns
Chip Select Recovery Time	t_{RCS}		1	3	5	1	3	5	ns
Address Access Time	t_{AA}		3	6.5	8	3	7.5	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	$t_{WSA}=3$ns	6	2	—	6	2	—	ns
Data Setup Time	t_{WSD}		1	0	—	1	0	—	ns
Data Hold Time	t_{WHD}		1	0	—	1	0	—	ns
Address Setup Time	t_{WSA}	$t_W=6$ns	3	0	—	3	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	2	0	—	ns
Chip Select Setup Time	t_{WSCS}		1	0	—	1	0	—	ns
Chip Select Hold Time	t_{WHCS}		1	0	—	1	0	—	ns
Write Disable Time	t_{WS}		1	3	5	1	3	5	ns
Write Recovery Time	t_{WR}		1	3	5	1	3	5	ns

3. RISE/FALL TIME

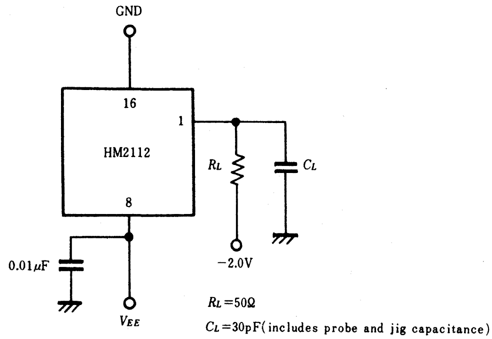
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		0.8	1.5	2.5	ns
Output Fall Time	t_f		0.8	1.5	2.5	ns

4. CAPACITANCE

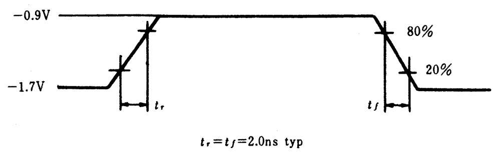
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		1	3	5	pF
Output Capacitance	C_{out}		3	5	8	pF

■ TEST CIRCUIT AND WAVEFORMS

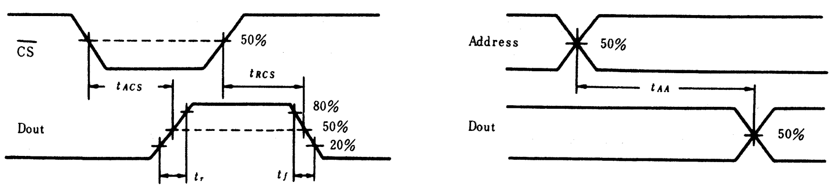
1. LOADING CONDITION



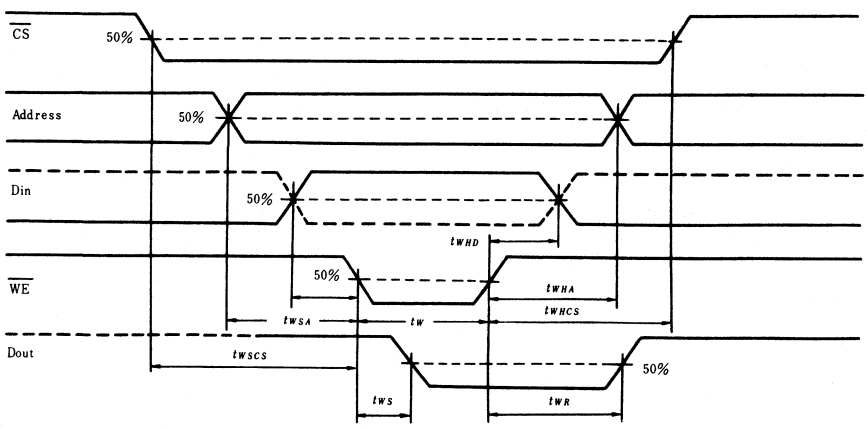
2. INPUT PULSE



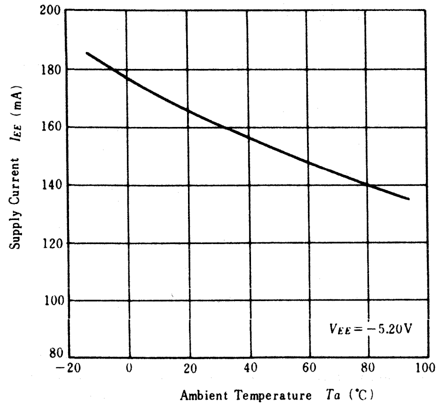
3. READ MODE



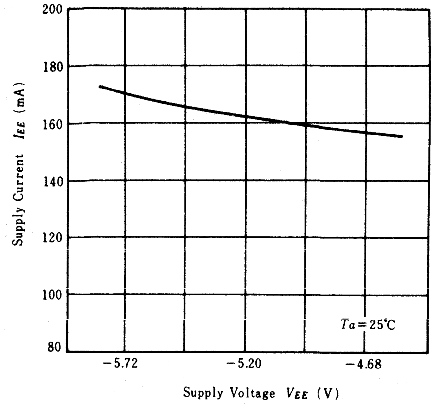
4. WRITE MODE



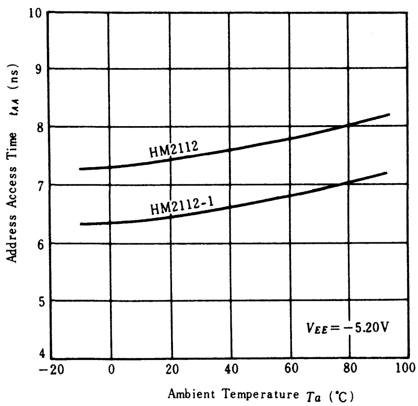
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



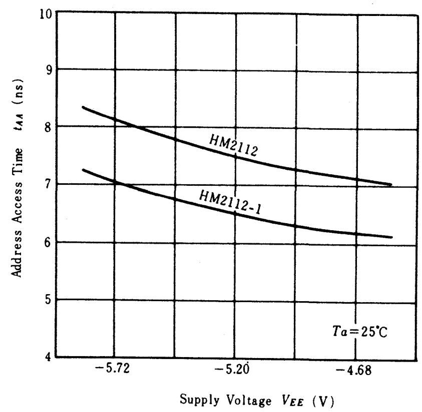
SUPPLY CURRENT vs. SUPPLY VOLTAGE



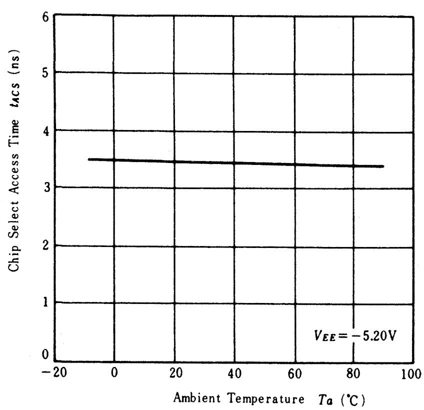
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



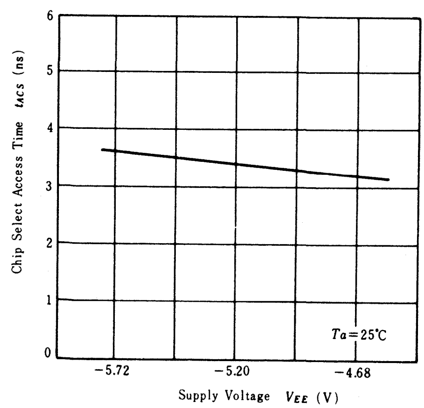
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



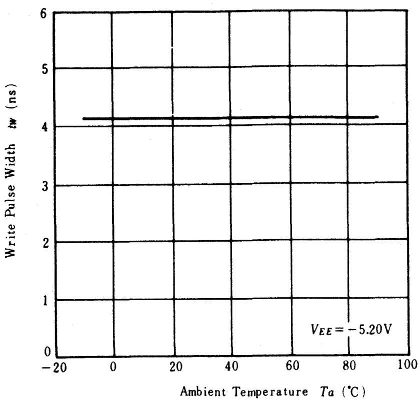
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



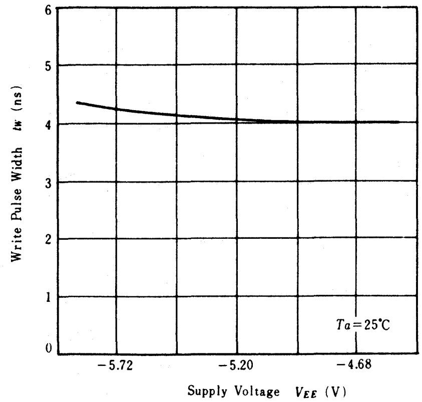
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



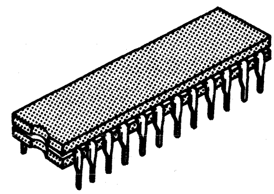
WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10422

256-word×4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.
Four active Low Block Select lines are provided to select each block independently.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.

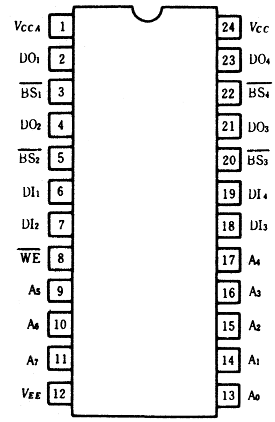


(DG-24A)

■FEATURES

- 256-word x 4 bit organization.
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns (min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■PIN ARRANGEMENT



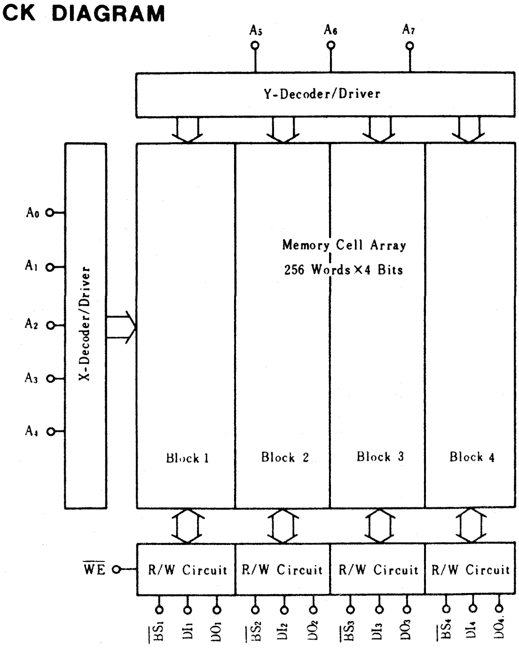
(Top View)

■TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read out noninvert

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

($V_{EE}=-5.2$V, $R_L=50\Omega$ to -2.0V, $Ta=0$ to $+75$°C, air flow exceeding 2m/sec)

●DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{BS}$ — $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other — $V_{IN}=V_{ILB}$	0 to +75°C	−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta=0°C	−200	−160	—	mA
			Ta=75°C	—	−145	—	

●AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	9	ns

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

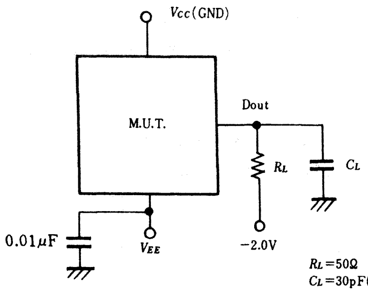
4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■TEST CIRCUIT AND WAVEFORMS

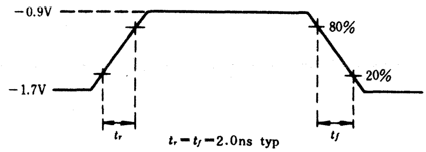
1. LOADING CONDITION

Test Circuit

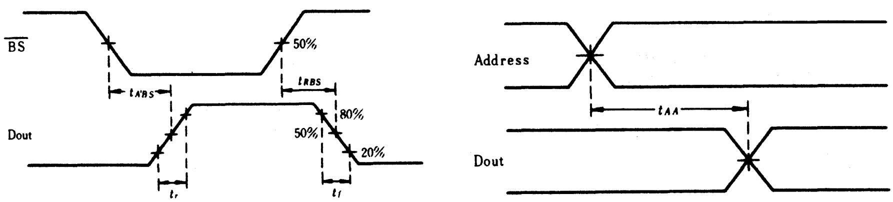


R_L=50Ω
C_L=30pF(includes probe and jig capacitance)

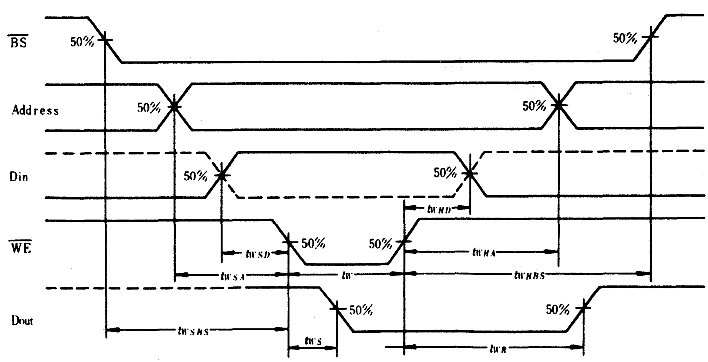
2. INPUT PULSE



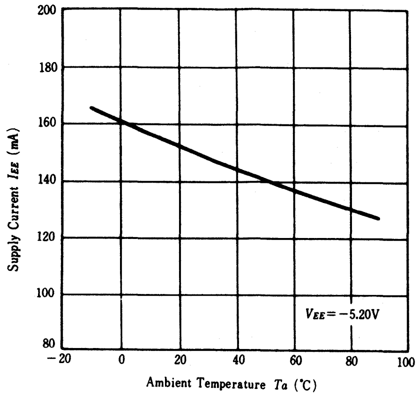
3. READ MODE



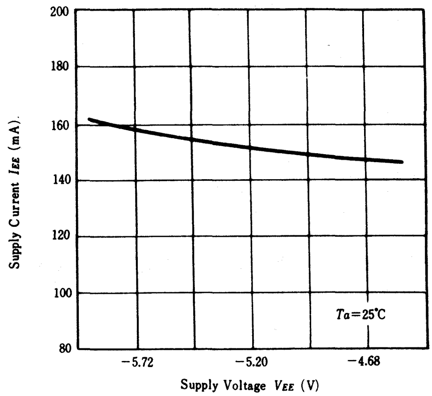
4. WRITE MODE



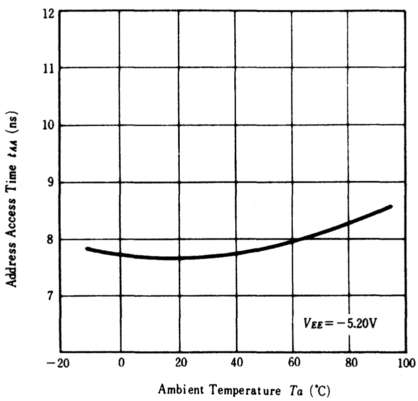
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



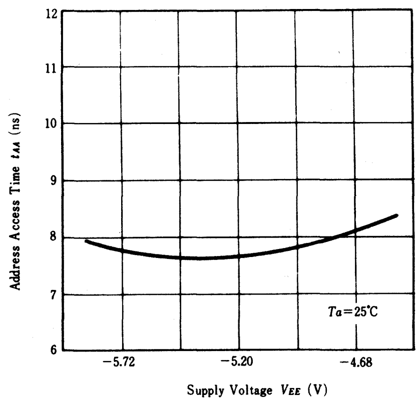
SUPPLY CURRENT vs. SUPPLY VOLTAGE



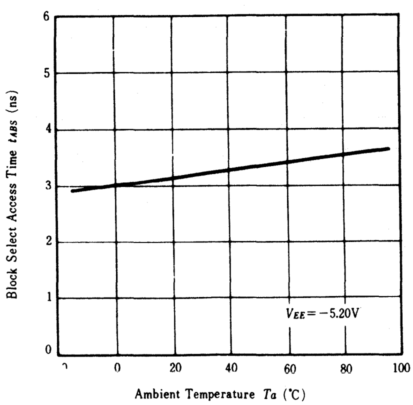
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



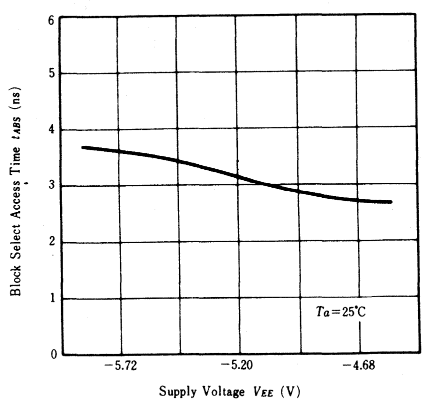
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



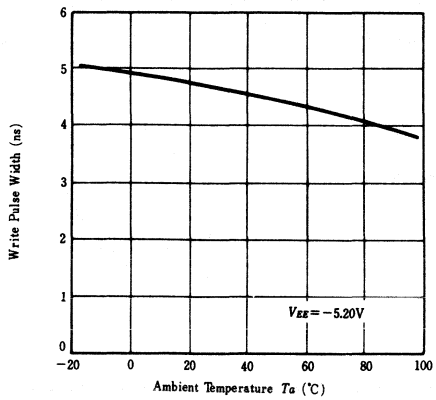
BLOCK SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



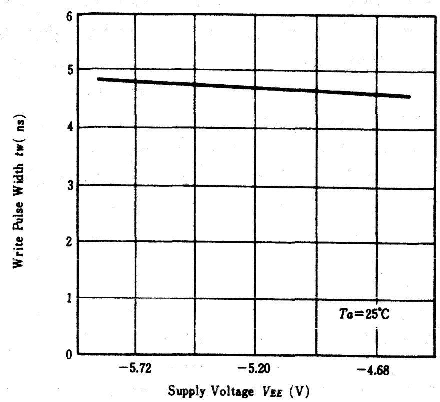
BLOCK SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



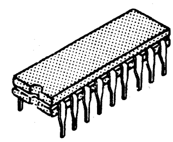
WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10470, HM10470-1

4096-word × 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10470 is encapsulated in cerdip-18pin package, compatible with Fairchild's F10470.

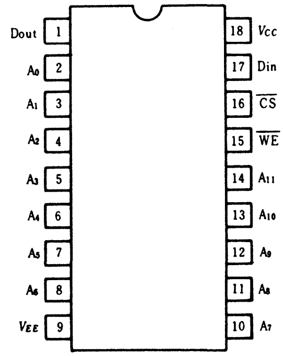


(DG-18)

■ FEATURES

- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10470 25ns (max)
  HM10470-1 15ns (max)
- Write pulse width: HM10470 25ns (min)
  HM10470-1 15ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



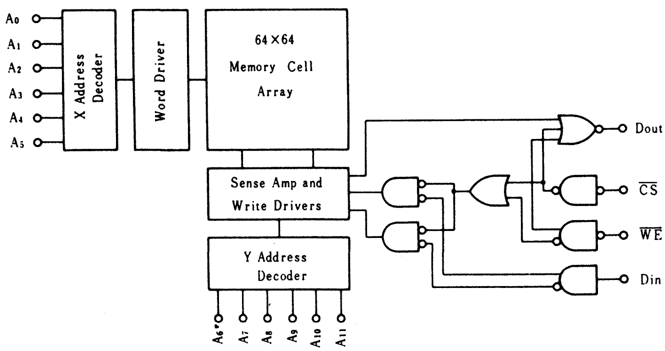
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS ($Ta=25°C$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ TEST CIRCUIT AND WAVEFORMS

● DC CHARACTERISTICS ($V_{EE}=-5.2$V, $R_L=50\Omega$ to -2.0V, $Ta=0$ to $+75$°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$, $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other, $V_{IN}=V_{ILB}$		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 9	$Ta=0$°C	−200*	−160*	—	mA
				−280**	−200**	—	
			$Ta=75$°C	—	−145	—	

* HM10470
** HM10470-1

● AC CHARACTERISTICS ($V_{EE}=-5.2$V ±5%, $Ta=0$ to $+75$°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	HM10470 min	HM10470 typ	HM10470 max	HM10470-1 min	HM10470-1 typ	HM10470-1 max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	—	—	8	ns
Address Access Time	t_{AA}		—	15	25	—	12	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10470 min	HM10470 typ	HM10470 max	HM10470-1 min	HM10470-1 typ	HM10470-1 max	Unit
Write Pulse Width	t_W	$t_{WSA}=3$ns	25	—	—	15	—	—	ns
Data Setup Time	t_{WSD}	$t_W=t_{W\,min}$	2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}		3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	8	ns

3. RISE/FALL TIME

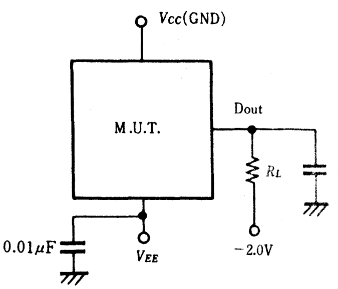
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

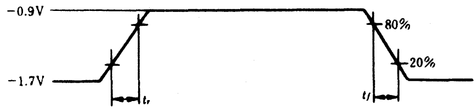
■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



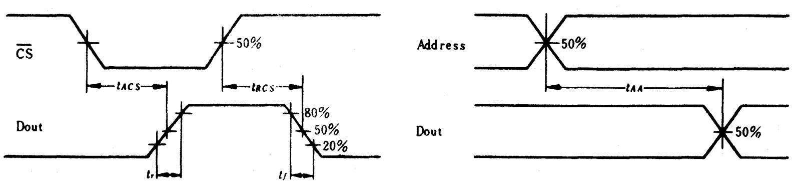
$R_L=50\Omega$
$C_L=30pF$ (includes probe and jig capacitance)

2. INPUT PULSE

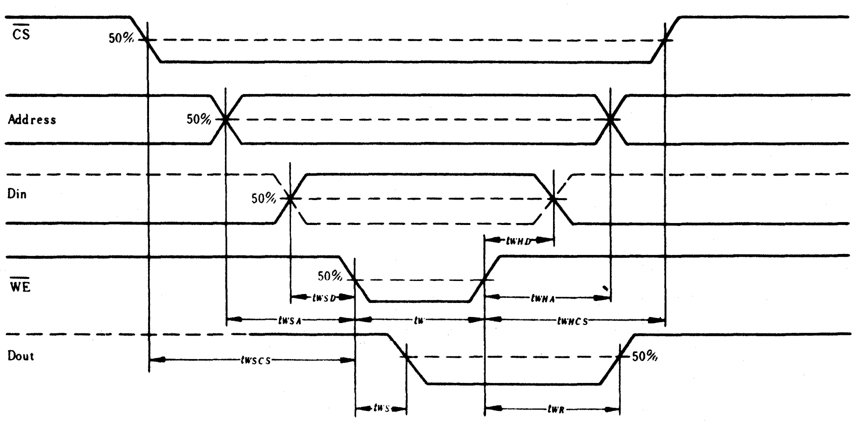


$t_r=t_f=2.0ns$ typ

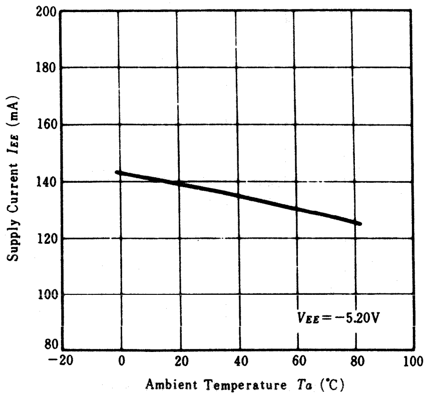
3. READ MODE



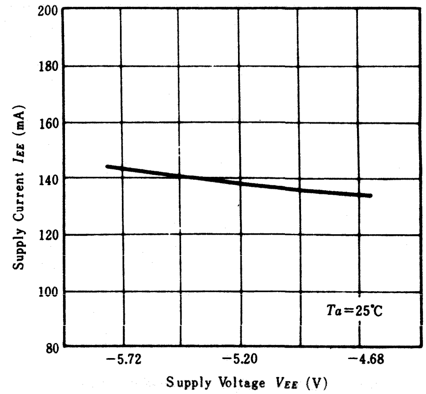
4. WRITE MODE



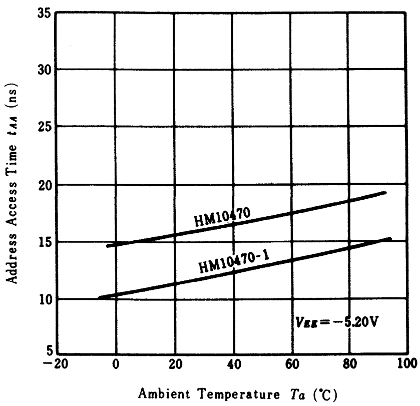
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



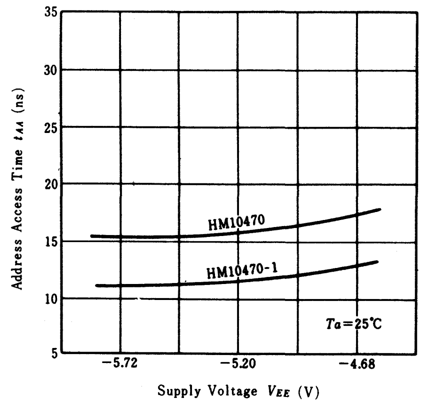
SUPPLY CURRENT vs. SUPPLY VOLTAGE



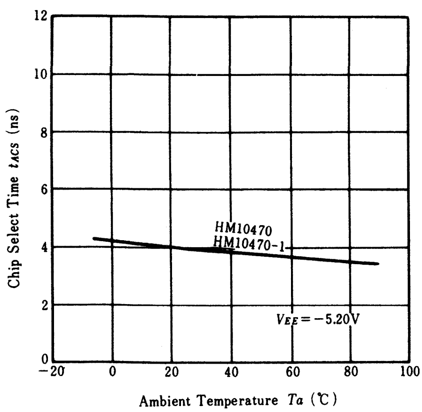
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



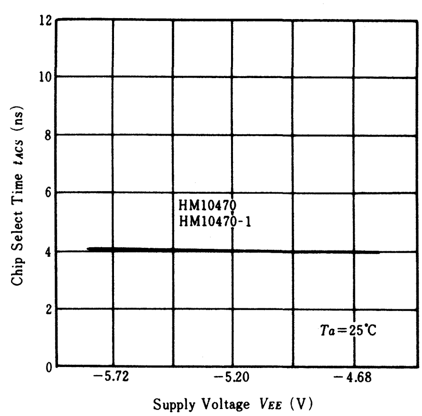
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



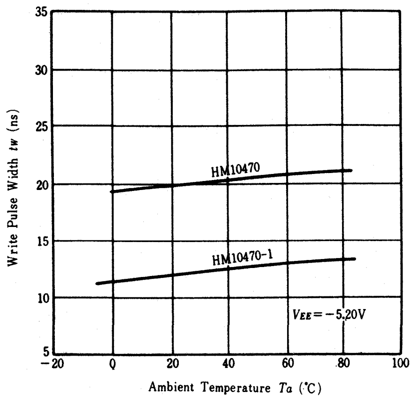
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



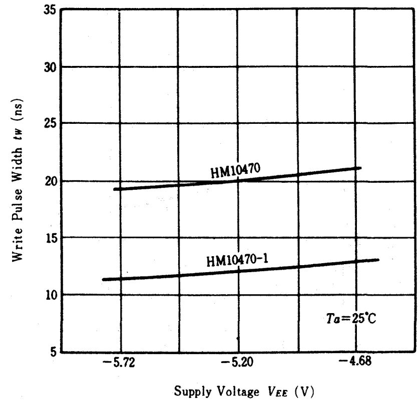
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



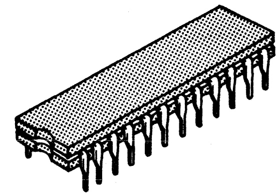
HM10474

1024-word×4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

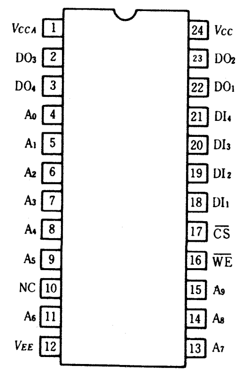


(DG-24A)

■ FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10k ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



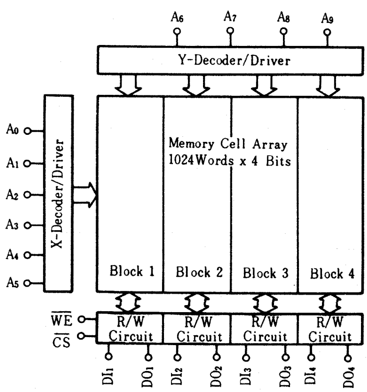
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS ($Ta=25°C$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS ($V_{EE}=-5.2$V, $R_L=50\Omega$ to -2.0V, $Ta=0$ to $+75$°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ ($V_{IN}=V_{ILB}$)	0 to +75°C	0.5	—	170	
		Others ($V_{IN}=V_{ILB}$)		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	$Ta=0$°C	−200	−160	—	mA
			$Ta=75$°C	—	−145	—	

●AC CHARACTERISTICS ($V_{EE}=-5.2$V ±5%, $Ta=0$ to $+75$°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=3$ns	25	15	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	$t_W=25$ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Ship Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

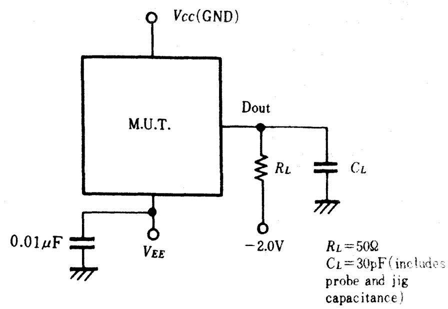
4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

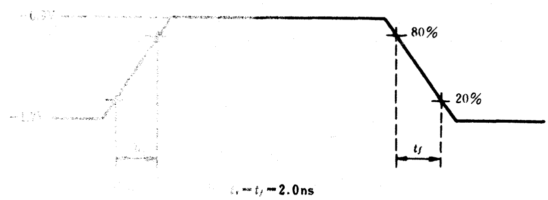
■TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

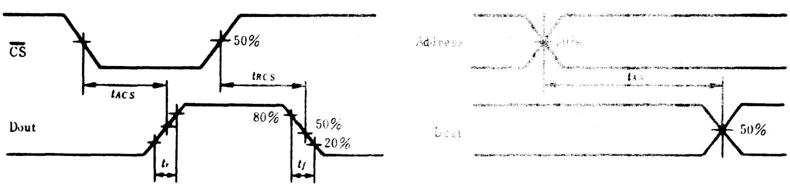
Test Circuit



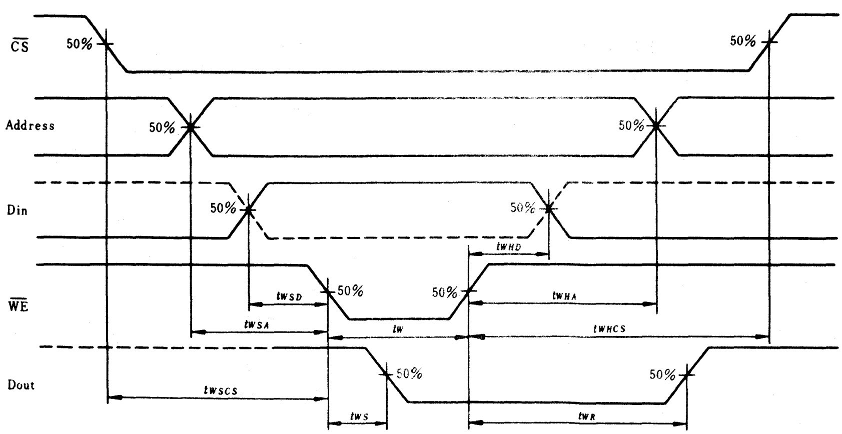
2. INPUT PULSE



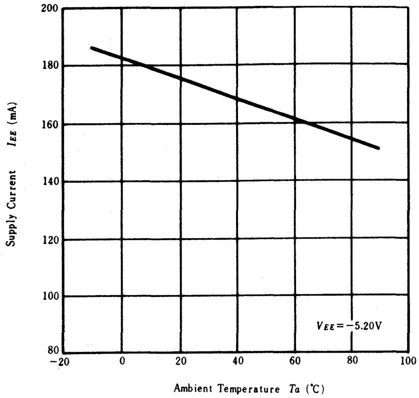
3. READ MODE



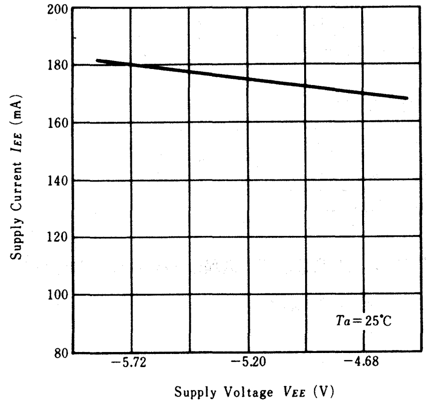
4. WRITE MODE



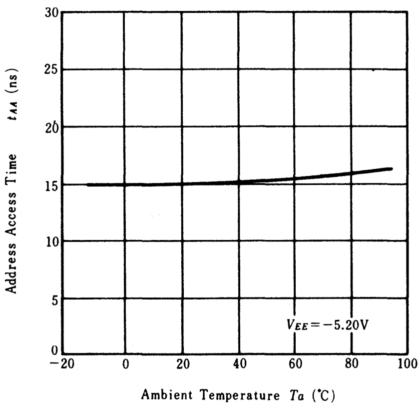
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



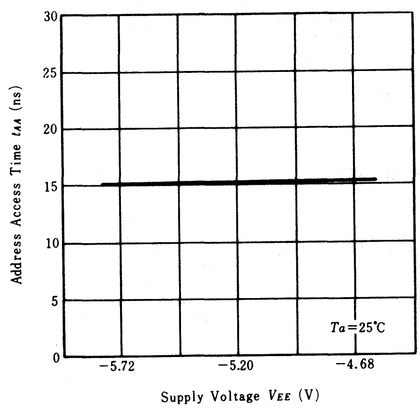
SUPPLY CURRENT vs. SUPPLY VOLTAGE



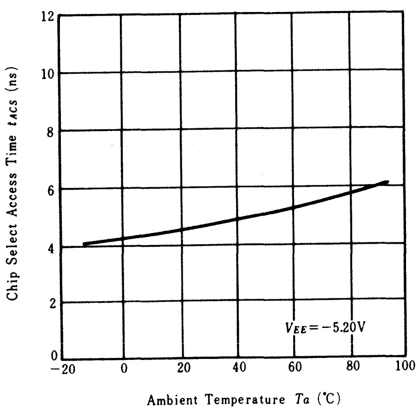
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



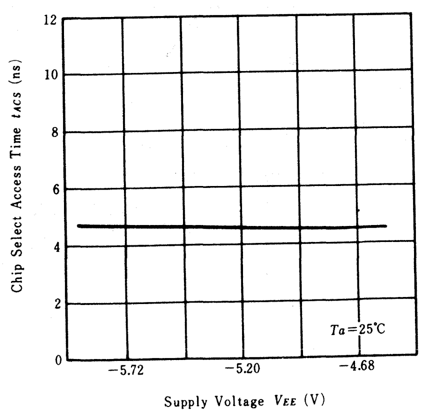
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



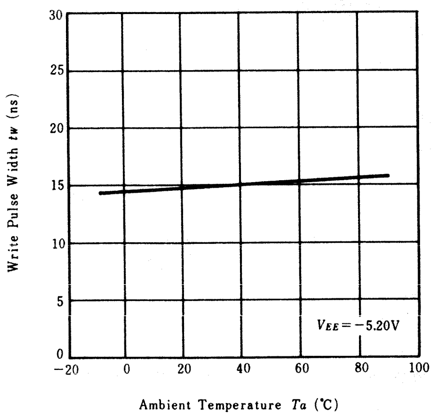
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



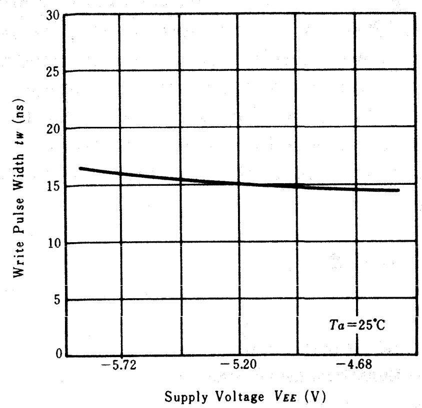
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



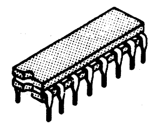
WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM100415

1024-word×1-bit Fully Decoded Random Access Memory

The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer storages which require very high speeds.
The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.

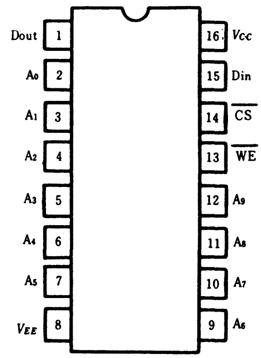


(DG-16A)

■ FEATURES

- Level .... 100K ECL Compatible
- Organization .... 1024-word by 1-bit
- Address Access Time .... 10ns (max)
- Chip Select Access Time .... 5ns (max.)
- Power Consumption .... 0.6mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Compatible with Fairchild F100415.

■ PIN ARRANGEMENT



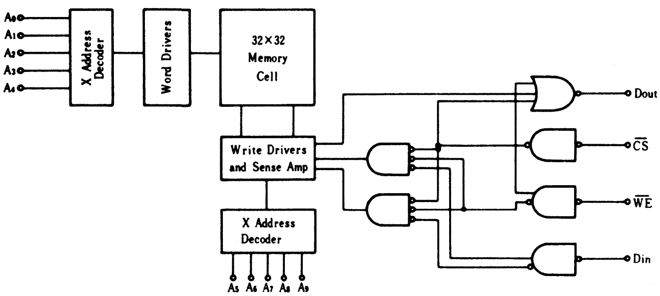
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS ($Ta=25^\circ C$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS ($V_{EE}=-4.5V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+85°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{in}=V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in}=V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in}=V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in}=V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−150	—	mA

●AC CHARACTERISTICS ($V_{EE}=-4.5V \pm 5\%$, $Ta=0$ to $+85°C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	3	5	ns
Chip Select Recovery Time	t_{RCS}		—	3	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=2ns$	6	4	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	$t_W=6ns$	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		2	0	—	ns
Chip Select Hold Time	t_{WHCS}		2	0	—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	5	ns

3. RISE/FALL TIME

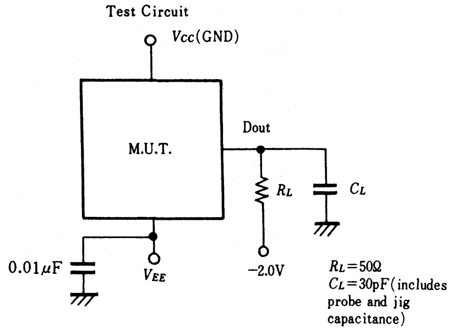
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

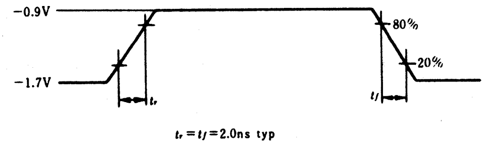
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

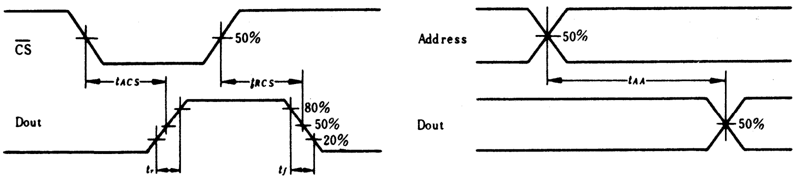
1. LOADING CONDITION



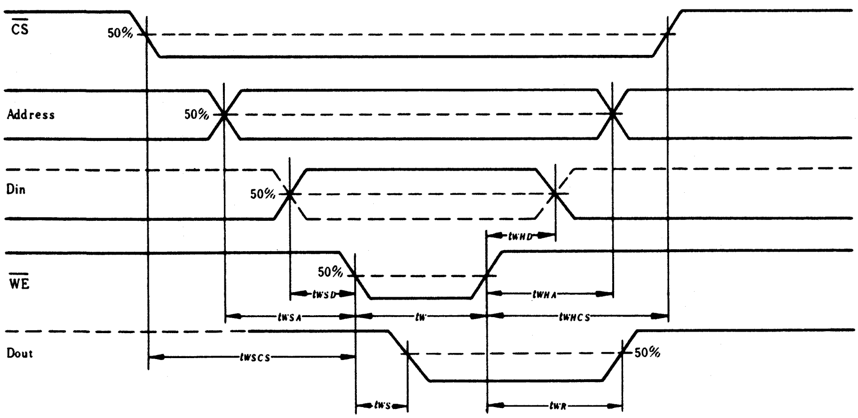
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100422, HM100422F

256-word×4-bit Fully Decoded Random Access Memory

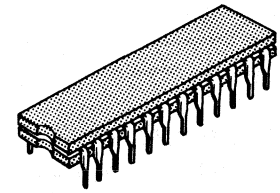
The HM100422 is ECL 100K compatible, 256-word x 4-bit, read write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

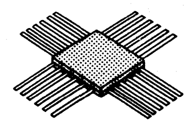
The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.

HM100422



(DG-24A)

HM100422F



(FG-24)

■ FEATURES

- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

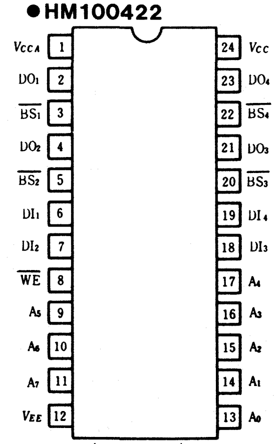
■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

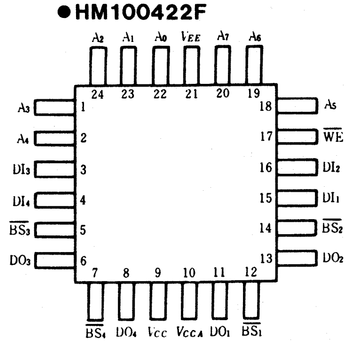
■ PIN ARRANGEMENT

● HM100422



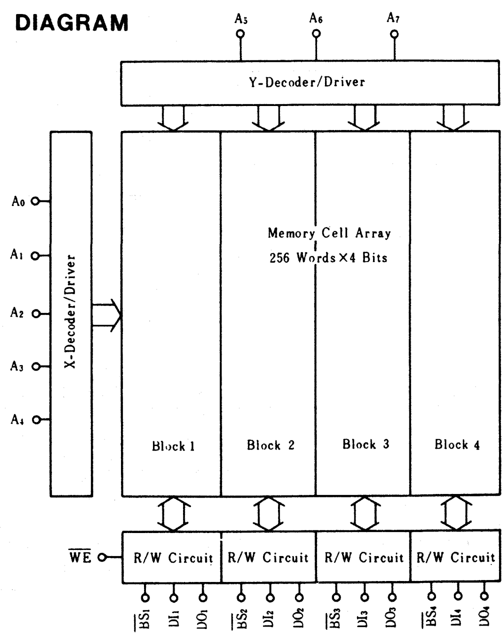
(Top View)

● HM100422F



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS ($Ta=25°C$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE}=-4.5V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+85°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{in}=V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in}=V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in}=V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in}=V_{ILB}$	$\overline{BS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

● AC CHARACTERISTICS ($V_{EE}=-4.5V \pm 5\%$, $Ta=0$ to $+85°C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=2ns$	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	$t_W=6ns$	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	9	ns

3. RISE/FALL TIME

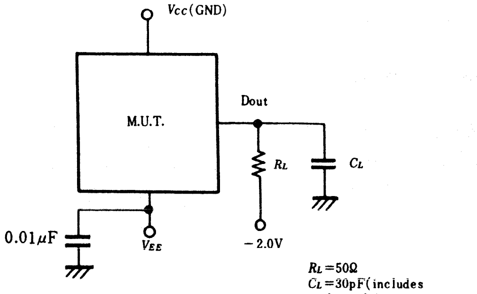
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

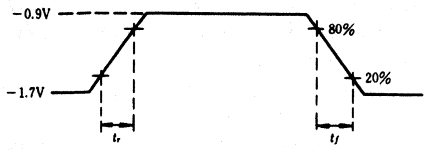
■ TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION



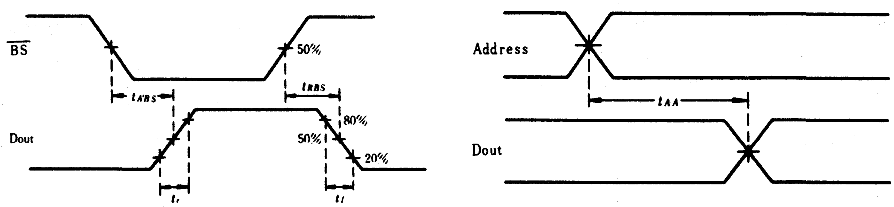
R_L = 50Ω
C_L = 30pF(includes probe and jig capacitance)

2. INPUT PULSE

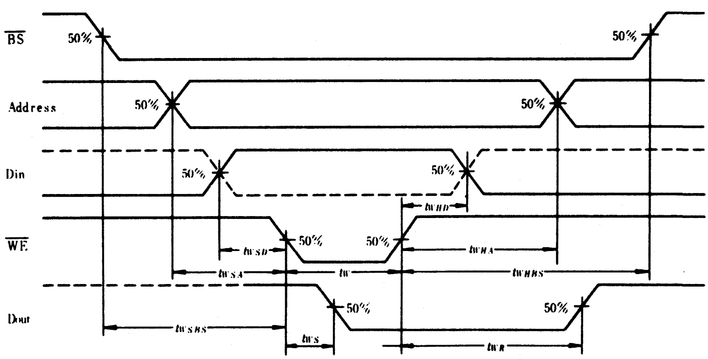


$t_r = t_f = 2.0$ns typ

3. READ MODE



4. WRITE MODE



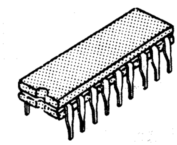
HM100470

4096-word × 1-bit Fully Decoded Random Access Memory

The HM100470 is a 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.

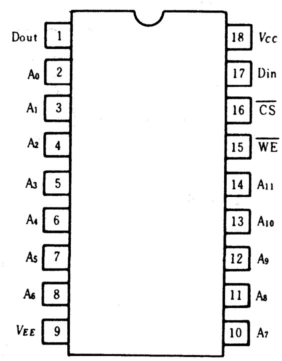


(DG-18)

■ FEATURES

- 4096-word x 1-bit organization
- Full compatible with 100k ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



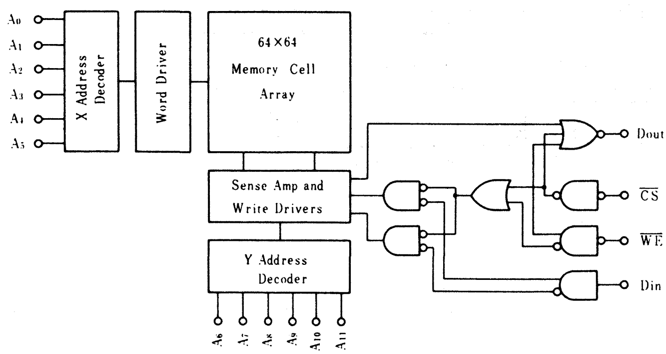
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS ($V_{EE}=-4.5$V, $R_L=50\Omega$ to -2.0V, $Ta=0$ to $+85$°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{in}=V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in}=V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in}=V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in}=V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS ($V_{EE}=-4.5$V ±5%, $Ta=0$ to $+85$°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	—	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=3$ns	25	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	$t_W=25$ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

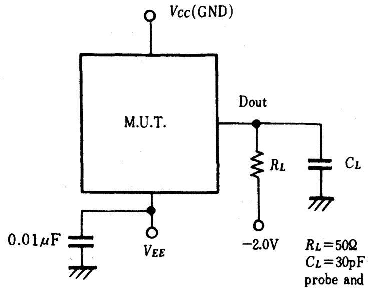
4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

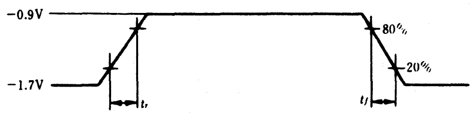
1. LOADING CONDITION

Test Circuit



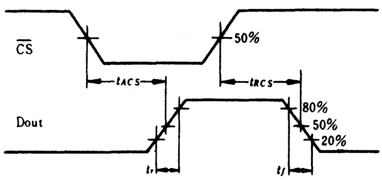
R_L=50Ω
C_L=30pF (includes probe and jig capacitance)

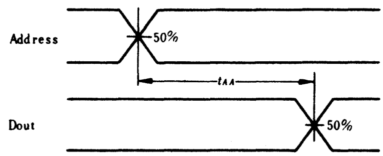
2. INPUT PULSE



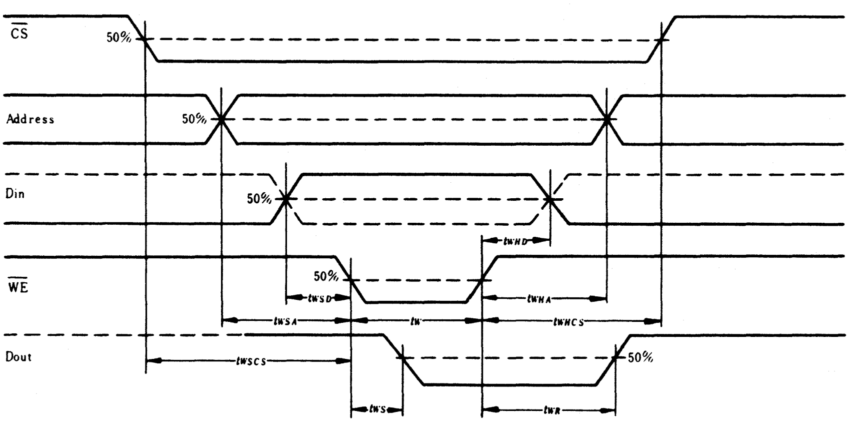
$t_r = t_f$ = 2.0ns typ

3. READ MODE





4. WRITE MODE

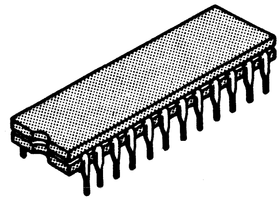


HM100474, HM100474F

1024-word×4-bit Fully Decoded Random Access Memory

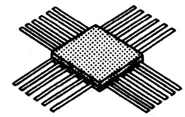
The HM100474 is a 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM100474 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-24-pin and flat 24pin package, compatible with Fairchild's F100474.

HM100474



(DG-24A)

HM100474F



(FG-24)

■ FEATURES

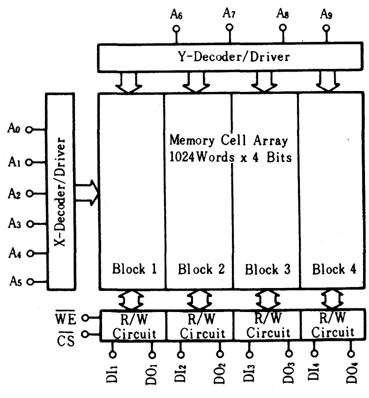
- 1024-word x 4-bit organization
- Fully compatible with 100k ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



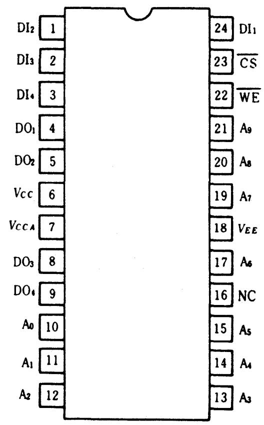
■ ABSOLUTE MAXIMUM RATINGS ($Ta=25°C$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

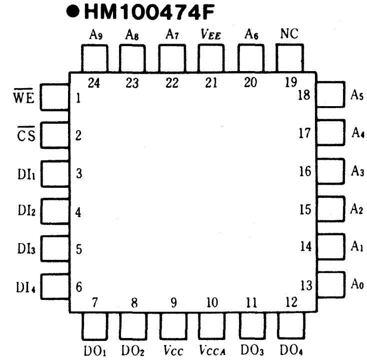
■ PIN ARRANGEMENT

● HM100474



(Top View)

● HM100474F



(Top View)

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in} = V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in} = V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in} = V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in} = V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=3ns	25	15	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W=25ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

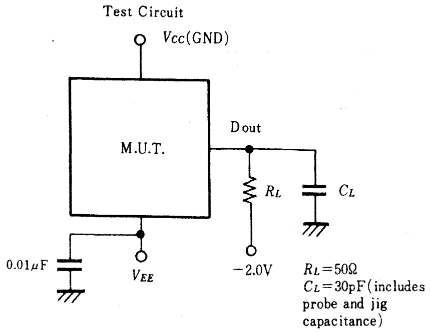
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

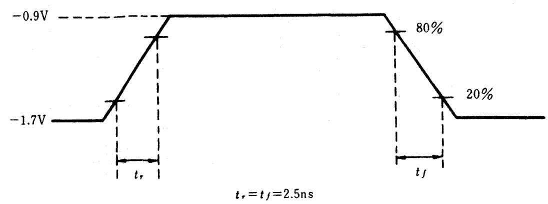
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

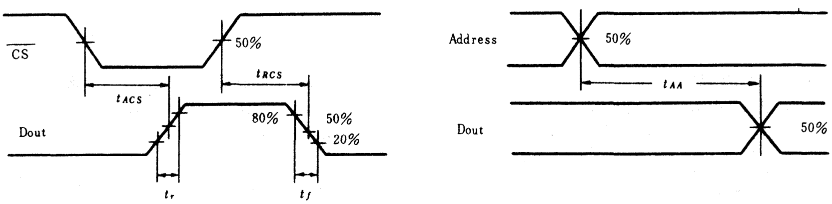
1. LOADING CONDITION



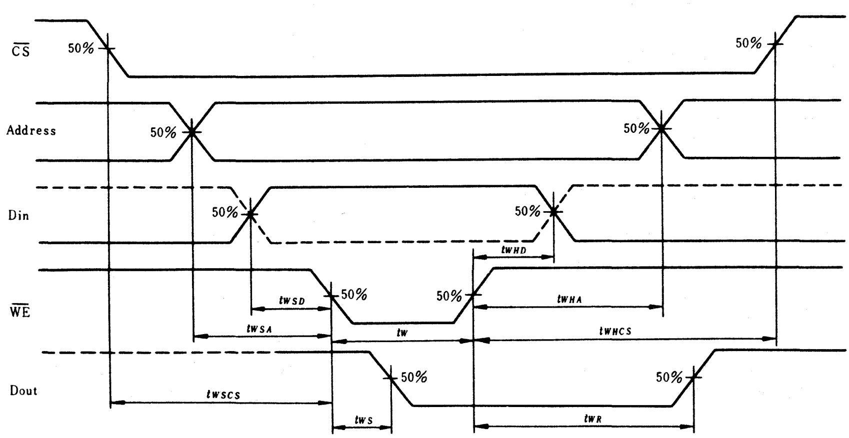
2. INPUT PULSE



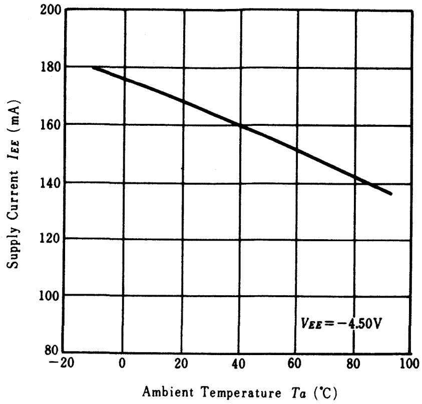
3. READ MODE



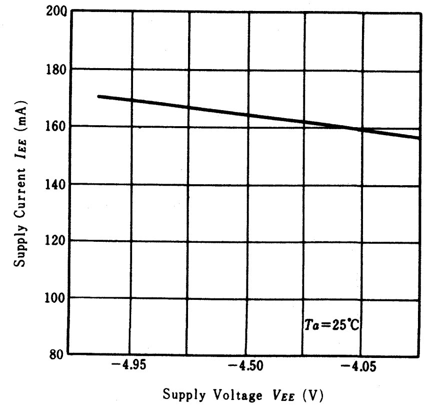
4. WRITE MODE



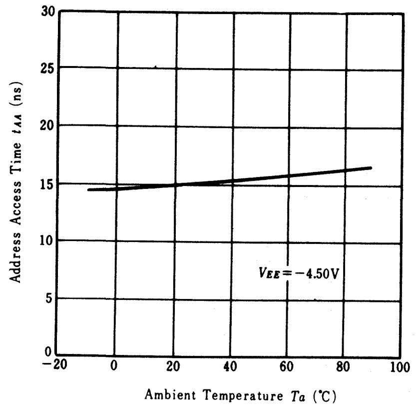
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



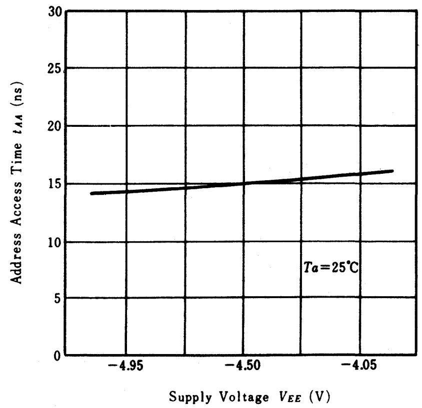
SUPPLY CURRENT vs. SUPPLY VOLTAGE



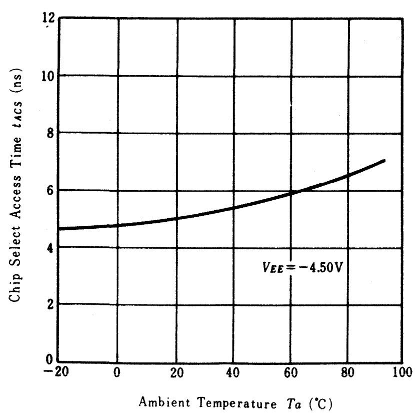
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



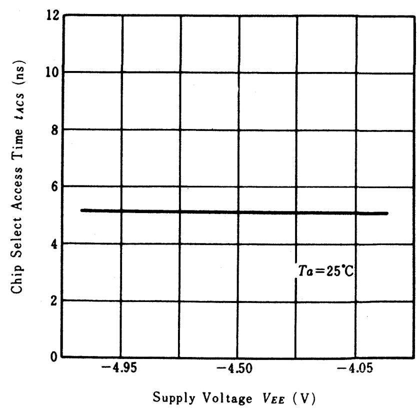
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



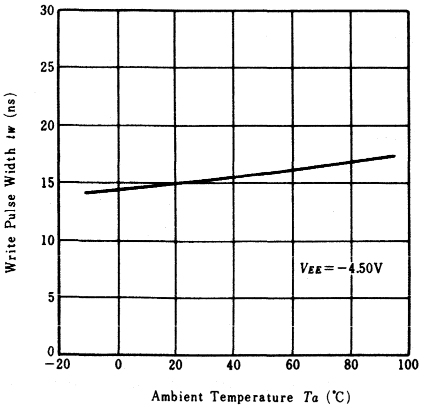
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



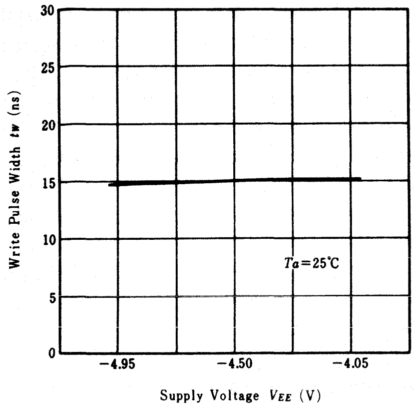
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

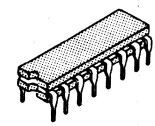


HM2504, HM2504-1

256-word×1-bit Fully Decoded Random Access Memory

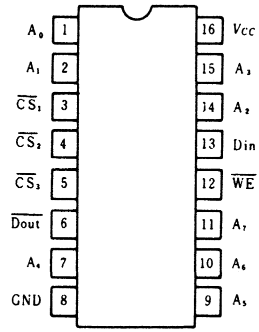
The HM2504 Series item is a TTL compatible, 256-word x 1-bit, read/write random access memory developed for application to buffer memories, control memories, high-speed main memories, etc. This is a fully decoded, read/write random access memory perfectly compatible with the standard DTL and TTL logic family, designed as an open collector output type for simplicity of expansion.

- Level .... TTL compatible
- Construction .... 256-word x 1 bit
- Read access time .... HM2504: 55ns (max)
  HM2504-1: 45ns (max.)
- Chip select access time .... 30ns (max.)
- Power consumption .... 1.8mW/bit (typ)
- Output .... Open collector



(DG-16)

■PIN ARRANGEMENT



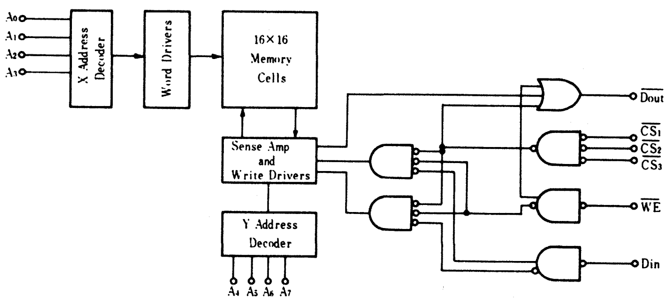
(Top View)

■TRUTH TABLE

Inputs			Output Open Collector	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	H	Not Selected
all L	L	L	H	Write "0"
all L	L	H	H	Write "1"
all L	H	×	$\overline{\text{Dout}}$*	Read

Notes) × : Don't care
* : Read out inverted

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2504, HM2504-1	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Input Current	I_{in}	−12 to +5.0	mA
Output Voltage (Output High)	V_{out}	−0.5 to +5.5	V
Output Voltage (DC Output Low)	I_{out}	+20	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{CC}=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		HM2504 Series			Unit
				min	typ	max	
Output Voltage	V_{OL}	V_{CC}=4.75V, I_{OL}=16mA		—	0.3	0.45	V
Input Voltage	V_{IH}	Guaranteed Input Voltage High		2.0	1.6	—	V
	V_{IL}	Guaranteed Input Voltage Low		—	1.5	0.85	V
Input Current	I_{IH}	V_{CC}=5.25V, V_{in}=4.5V		—	0	20	μA
	I_{IL}	V_{CC}=5.25V, V_{in}=0		—	−530	−800	μA
Output Leakage Current	I_{CEX}	V_{CC}=5.25V, V_{out}=4.5V		—	0	50	μA
Input Clamp Voltage	V_I	V_{CC}=5.25V, I_{in}=−10mA		—	−1.0	−1.5	V
Supply Current	I_{CC}	V_{CC}=5.25V All input GND	0< Ta <25°C	—	—	135	mA
			Ta ≧25°C	—	—	130	mA

●AC CHARACTERISTICS

(V_{CC}=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/s, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2504			HM2504-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	12	30	—	12	30	ns
Chip Select Recovery Time	t_{RCS}		—	18	25	—	18	25	ns
Address Access Time	t_{AA}		—	35	55	—	30	45	ns

2. WRITE MODE

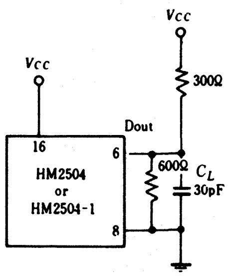
Item	Symbol	Test Condition	HM2504			HM2504-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA}=0ns	30	8	—	30	8	—	ns
Data Setup Time	t_{WSD}		0	0	—	0	0	—	ns
Data Hold Time	t_{WHD}		5	0	—	5	0	—	ns
Address Setup Time	t_{WSA}	t_W=30ns	0	0	—	0	0	—	ns
Address Hold Time	t_{WHA}		5	0	—	5	0	—	ns
Chip Select Setup Time	t_{WSCS}		0	0	—	0	0	—	ns
Chip Select Hold Time	t_{WHCS}		5	0	—	5	0	—	ns
Write Disable Time	t_{WS}		—	14	35	—	14	35	ns
Write Recovery Time	t_{WR}		—	12	40	—	12	40	ns

3. CAPACITANCE

Item	Symbol	Test Condition	HM2504			HM2504-1			Unit
			min	typ	max	min	typ	max	
Input Capacitance	C_{in}		—	3	5	—	3	5	pF
Output Capacitance	C_{out}		—	6	8	—	6	8	pF

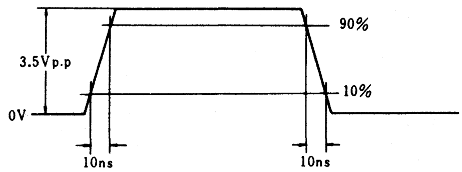
TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

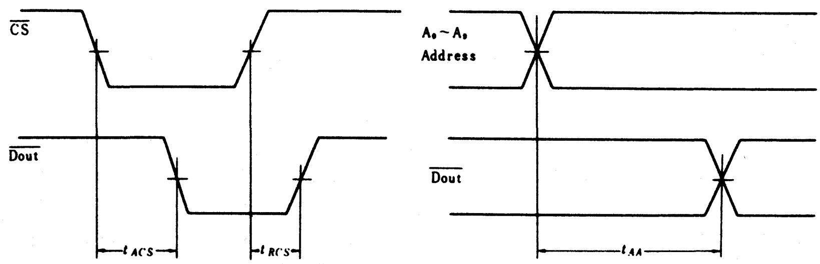


Note: C_L includes jig and stray capacitance

2. INPUT PULSE

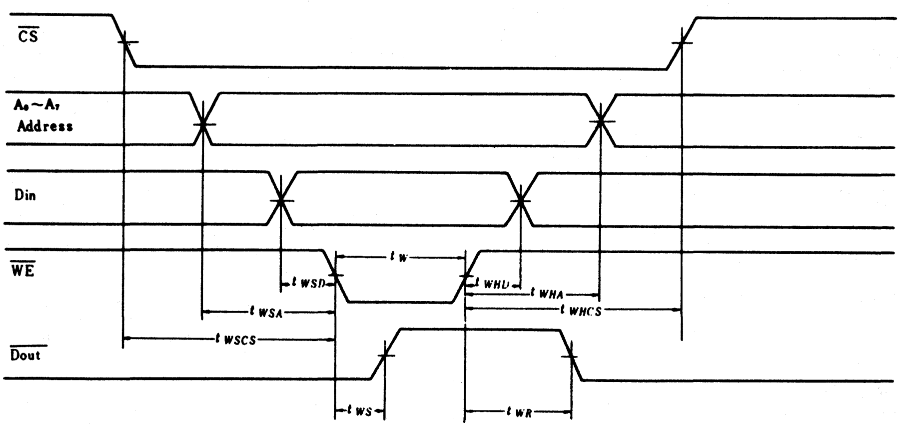


3. READ MODE



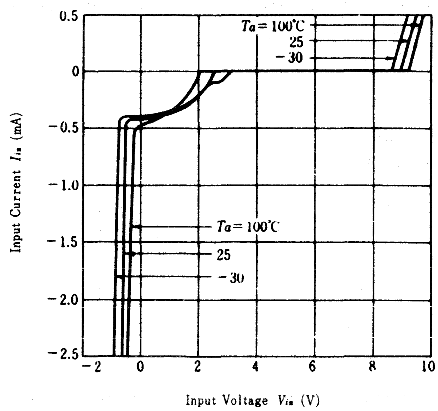
(All time measurements refer to 1.5V)

4. WRITE MODE

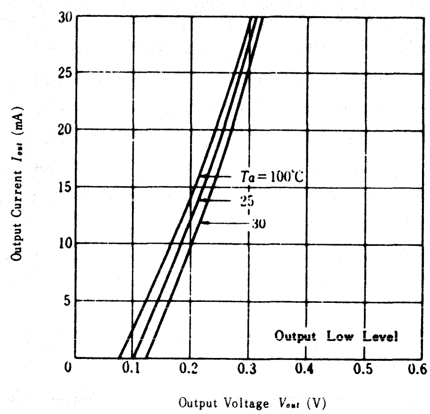


(All time measurements refer to 1.5V)

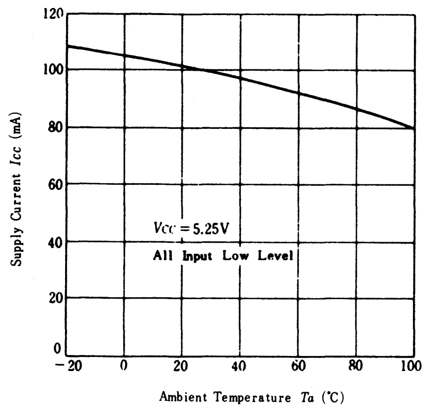
INPUT CHARACTERISTICS



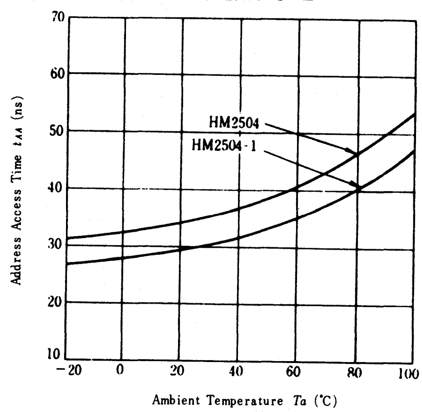
OUTPUT CHARACTERISTICS



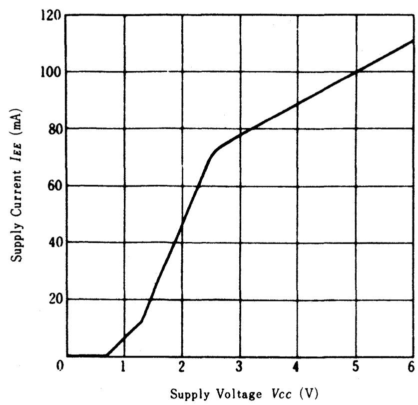
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

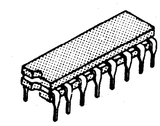


HM2510, HM2510-1, HM2510-2

1024-word × 1-bit Fully Decoded Random Access Memory

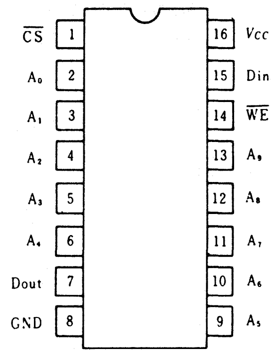
The HM2510 Series item is a 1024-word x 1-bit read/write random access memory developed for application to buffer memories, control memories, high-speed main memories, etc. It is a fully decoded, read write, random access memory perfectly compatible with standard DTL and TTL logic families, designed as an open collector output type for simplicity of expansion.

- Level .... TTL compatible
- Construction .... 1024-word x 1 bit
- Read access time .... HM2510: 70ns (max.)
  HM2510-1: 45ns (max)
  HM2510-2: 35ns (max.)
- Chip select access time .... HM2510: 40ns (max.)
  HM2510-1: 30ns (max.)
  HM2510-2: 25ns (max.)
- Power consumption 0.5mW/bit
- Output .... Open collector



(DG-16A)

■ PIN ARRANGEMENT



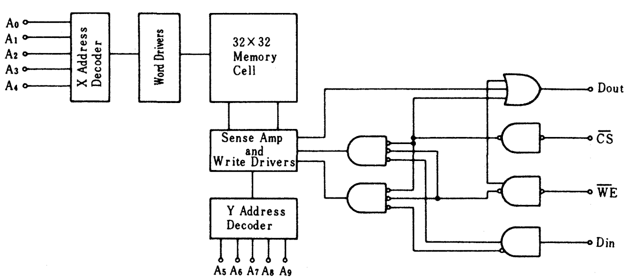
(Top View)

■ TRUTH TABLE

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	×	Dout*	Read

Notes) × : Don't care
* : Read out non-inverted

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2510 Series	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Input Current	I_{in}	−12 to +5.0	mA
Output Voltage (Output High)	V_{out}	−0.5 to +5.5	V
Output Voltage (DC Output Low)	I_{out}	+20	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{CC}=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		HM2510 Series			Unit
				min	typ	max	
Output Voltage	V_{OL}	V_{CC}=4.75V, I_{OL}=16mA		—	0.3	0.45	V
Input Voltage	V_{IH}	Guaranteed Input Voltage High		2.1	1.6	—	V
	V_{IL}	Guaranteed Input Voltage Low		—	1.5	0.80	V
Input Current	I_{IH1}	V_{CC}=5.25V, V_{in}=4.5V		—	0	40	μA
	I_{IH2}	V_{CC}=5.25V, V_{in}=5.25V		—	0	1.0	mA
	I_{IL}	V_{CC}=5.25V, V_{in}=0.4V		—	−250	−400	μA
Output Leakage Current	I_{CEX}	V_{CC}=5.25V, V_{out}=4.5V		—	0	100	μA
Input Clamp Voltage	V_I	V_{CC}=5.25V, I_{in}=−10mA		—	−1.1	−1.5	V
Supply Current	I_{CC}	V_{CC}=5.25V All input GND	0< Ta<25°C	—	—	155	mA
			Ta≧25°C	—	95	130	mA

● AC CHARACTERISTICS (V_{CC}=5.0V ±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM2510			HM2510-1			HM2510-2			Unit
			min	typ	max	min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	15	40	—	—	30	—	15	25	ns
Chip Select Recovery Time	t_{RCS}		—	25	40	—	—	30	—	17	25	ns
Address Access Time	t_{AA}		—	40	70	—	35	45	—	25	35	ns

2. WRITE MODE

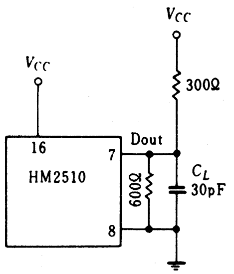
Item	Symbol	Test Condition	HM2510			HM2510-1			HM2510-2			Unit
			min	typ	max	min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA}=min	50	10	—	35	10	—	25	10	—	ns
Data Setup Time	t_{WSD}		5	0	—	5	—	—	5	0	—	ns
Data Hold Time	t_{WHD}		5	0	—	5	—	—	5	0	—	ns
Address Setup Time	t_{WSA}	t_W=min	15	0	—	5	—	—	5	0	—	ns
Address Hold Time	t_{WHA}		5	0	—	5	—	—	5	0	—	ns
Chip Select Setup Time	t_{WSCS}		5	0	—	5	—	—	5	0	—	ns
Chip Select Hold Time	t_{WHCS}		5	0	—	5	—	—	5	0	—	ns
Write Disable Time	t_{WS}		—	20	40	—	20	35	—	15	25	ns
Write Recovery Time	t_{WR}		—	30	55	—	30	45	—	15	25	ns

3. CAPACITANCE

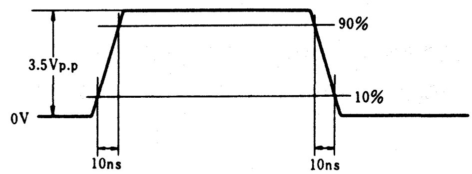
Item	Symbol	Test Condition	HM2510 Series			Unit
			min	typ	max	
Input Capacitance	C_{in}		—	3	5	pF
Output Capacitance	C_{out}		—	6	8	pF

■ TEST CIRCUIT AND WAVEFORMS

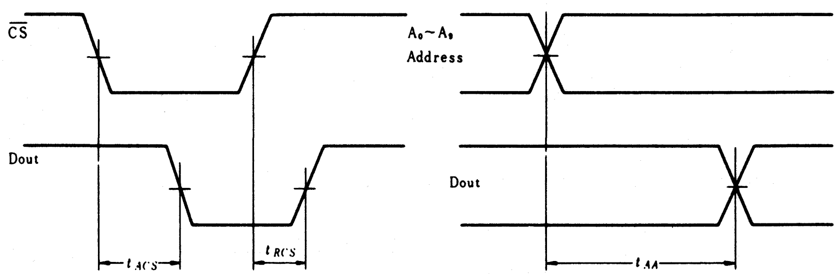
1. LOADING CONDITION



2. INPUT PULSE

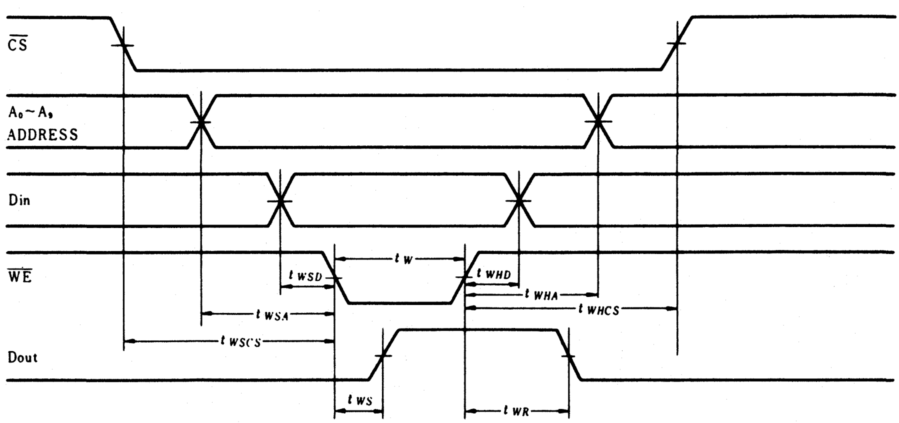


3. READ MODE



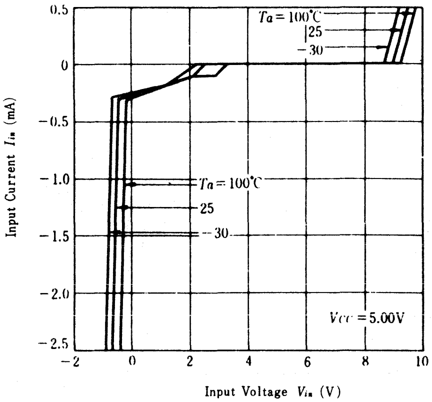
(All time measurements refer to 1.5V)

4. WRITE MODE

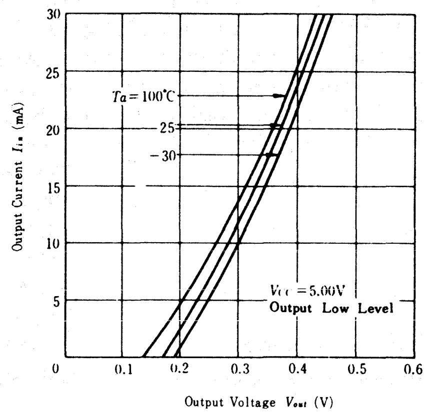


(All time measurements refer to 1.5V)

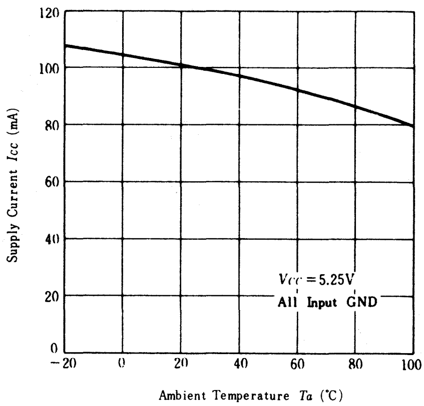
INPUT CHARACTERISTICS



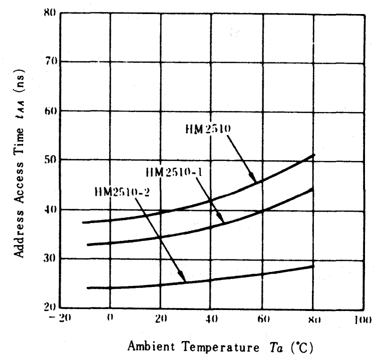
OUTPUT CHARACTERISTICS



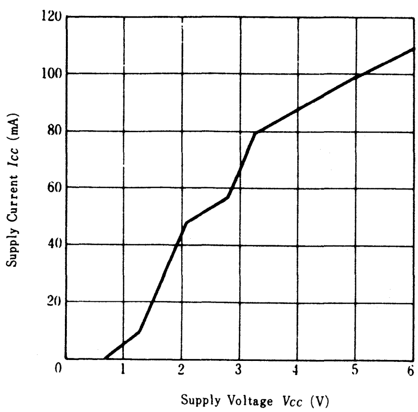
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

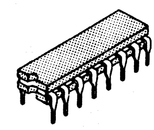


HM2511, HM2511-1

1024-word × 1-bit Fully Decoded Random Access Memory

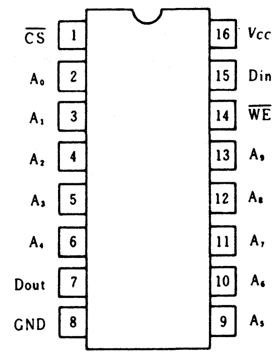
The HM2511 Series item is a 1024-word x 1-bit read/write random access memory with three-state output developed for application to buffer memories, control memories, high-speed main memories, etc. It is a fully decoded, read/write, random access memory perfectly compatible with standard DTL and TTL logic families.

- Level .... TTL compatible
- Construction .... 1024-word x 1 bit
- Read access time .... HM2511: 70ns (max)
  HM2511-1: 45ns (max)
- Chip select access time .... HM2511: 40ns (max)
  HM2511-1: 30ns (max)
- Power consumption 0.5mW/bit
- Output .... three-state



(DG-16A)

■ PIN ARRANGEMENT



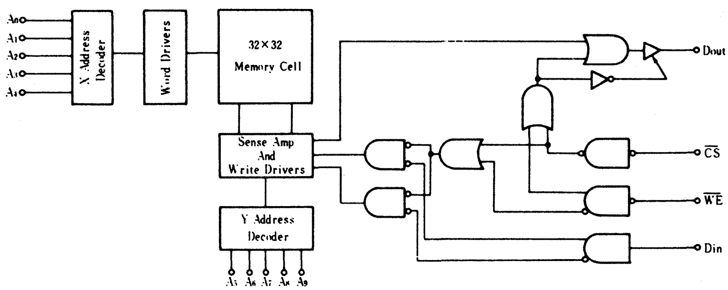
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	×	Dout*	Read

Notes) × : Don't care
* : Read out noninverted

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2511 Series	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Input Current	I_{in}	−12 to +5.0	mA
Output Voltage (Output High)	V_{out}	−0.5 to +5.5	V
Output Voltage (DC Output Low)	I_{out}	+20	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{CC}=5.0V ±5%, Ta=0 to +75℃, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		HM2511 Series			Unit
				min	typ	max	
Output Low Voltage	V_{OL}	V_{CC}=4.75V, I_{OL}=16mA		—	0.3	0.45	V
Input Voltage	V_{IH}	Guaranteed Input Voltage High		2.1	1.6	—	V
	V_{IL}	Guaranteed Input Voltage Low		—	1.5	0.8	V
Input Current	I_{IH1}	V_{CC}=5.25V, V_{in}=4.5V		—	0	40	μA
	I_{IH2}	V_{CC}=5.25V, V_{in}=5.25V		—	0	1.0	mA
	I_{IL}	V_{CC}=5.25V, V_{in}=0.4V		—	−250	−400	μA
Output Current (High Z)	I_{OFF1}	V_{CC}=5.25V, V_{out}=2.4V		—	—	50	μA
	I_{OFF2}	V_{CC}=5.25V, V_{out}=0.5V		—	—	−50	μA
Output Current Short Circuit to Ground	I_{OS}	V_{CC}=5.25V,		—	—	−100	mA
Output High Voltage	V_{OH}	I_{OH}=−10.3mA, V_{CC}=5.0V ±5%		2.4	—	—	V
Input Clamp Voltage	V_I	V_{CC}=5.25V, I_{in}=−10mA		—	−1.0	−1.5	V
Supply Current	I_{CC}	V_{CC}=5.25V All input GND	0≦Ta<25℃	—	—	155	mA
			Ta≧25℃	—	95	130	mA

●AC CHARACTERISTICS (V_{CC}=5.0V ±5%, Ta=0 to +75℃, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM2511			HM2511-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	15	40	—	—	30	ns
Chip Select to High Z	t_{ZRCS}		—	20	40	—	—	30	ns
Address Access Time	t_{AA}		—	40	70	—	35	45	ns

2. WRITE MODE

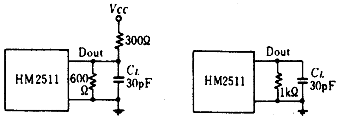
Item	Symbol	Test Condition	HM2511			HM2511-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA}=min	50	25	—	35	10	—	ns
Data Setup Time	t_{WSD}		5	0	—	5	—	—	ns
Data Hold Time	t_{WHD}		5	0	—	5	—	—	ns
Address Setup Time	t_{WSA}	t_W=min	15	0	—	5	—	—	ns
Address Hold Time	t_{WHA}		5	0	—	5	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	0	—	5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	0	—	5	—	—	ns
Write Disable to High Z	t_{ZWS}		—	20	40	—	20	35	ns
Write Recovery Time	t_{WR}		—	42	55	—	30	45	ns

3. CAPACITANCE

Item	Symbol	Test Condition	HM2511 Series			Unit
			min	typ	max	
Input Capacitance	C_{in}		—	3	5	pF
Output Capacitance	C_{out}		—	9	11	pF

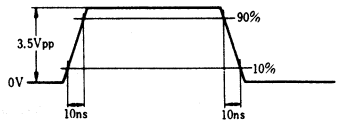
TEST CIRCUIT AND WAVEFORMS

1. LOADING CONDITION

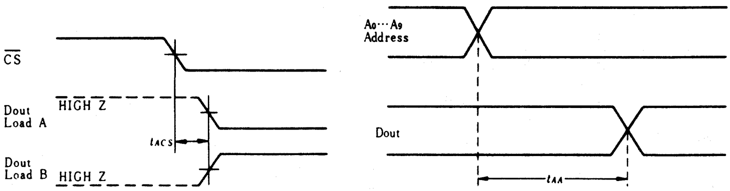


Load A　　Load B

2. INPUT PULSE

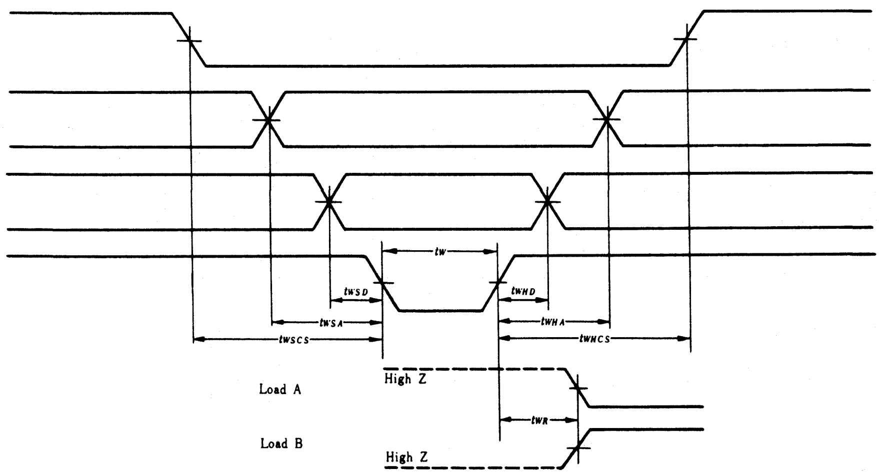


3. READ MODE



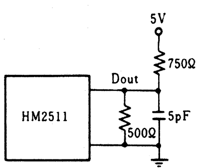
(All time measurements refer to 1.5V)

4. WRITE MODE

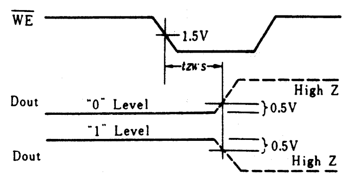


(All time measurements refer to 1.5V)

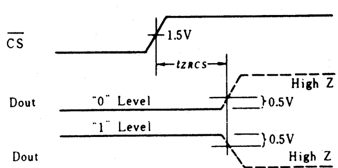
5. WRITE ENABLE TO HIGH Z DELAY



Load C



6. PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{Zxxx} parameters are measured at a delta of 0.5V from the logic level and using Load C)

BIPOLAR PROM

■ PROGRAMMING INFORMATION

Hitachi's sophisticated Fine Emitter technology and programming pulse method enables higher programmability and faster programming time ordinary PROMs, for the highest reliability.

Fast programming time of typically 7.5μs/bit is achieved with a fine emitter cell which requires less programming energy; thus, negligible thermal stress. Further, Hitachi advanced technology allows very high programmability.

To assure that the element is programmed properly an additional four programming pulses are applied immediately after a sense pulse indicates conduction in the programmed (one programming pulse: Series) bit. This high reliability feature virtually eliminates aluminum migration in the programmed cell.

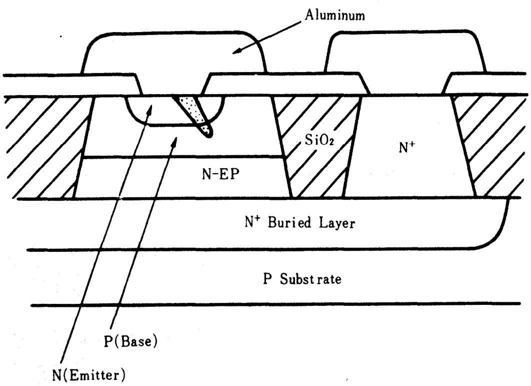
One extra row and one extra column of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and eliability.

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

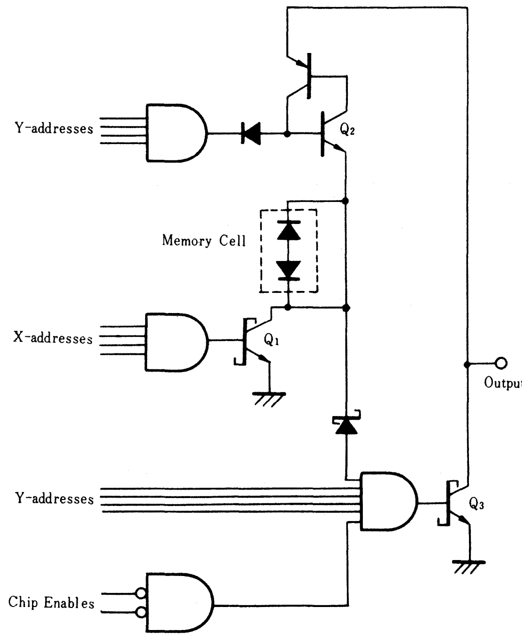
A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using ten address inputs to turn on transistors Q1 and Q2. By taking either (or both) chip enable inputs high, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the sensed voltage indicates that the selected bit is in the logic in state.

An additional 4 programming pulses (1 programming pulse: S-series) are required to ensure that the bit is fully programmed, and to achieve high reliability. One output must be programmed at a time, since the internal decording circuit is capable of sinking only one unit of programming current at time.

PROGRAMMED CELL (CROSS SECTION)



INTERNAL PROGRAMMING CIRCUIT



■HITACHI PROMS AND PROGRAMMING CURRENT

Memory Size	Organization	Output	N-Series	S-Series
4k	1k×4	O.C.	HN25044 (50ns max)	—
		3S	HN25045 (50ns max)	—
8k	2k×4	O.C.	HN25084 (60ns max)	HN25084S (50ns max)
		3S	HN25085 (60ns max)	HN25085S (50ns max)
	1k×8	O.C.	HN25088 (60ns max)	HN25088S (50ns max)
		3S	HN25089 (60ns max)	HN25089S (50ns max)
16k	2k×8	O.C.	—	HN25168S (60ns max)
		3S	—	HN25169S (60ns max)
Programming Current			130mA (typ)	90mA (typ)

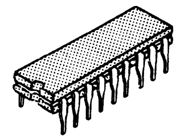
Note) O.C. : Open Collector Output
3 S : Three State Output

Hitachi's PROM has two families in accordance with the program specifications. They are usually discriminated by the suffix of the model name. For the S-series PROM, the production technique established for the N-series PROM is further improved to attain very small memory cell area and chip area as well as high performance.

HN25044, HN25045

1024-word × 4-bit Programmable Read Only Memory

The HITACHI HN25044 and HN25045 are high speed electrically programmable, fully decoded TTL Bipolar 4096 bit read only memories organized at 1024 words by 4 bits with on-chip address decoding and two chip enable inputs. The HN25044 and HN25045 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

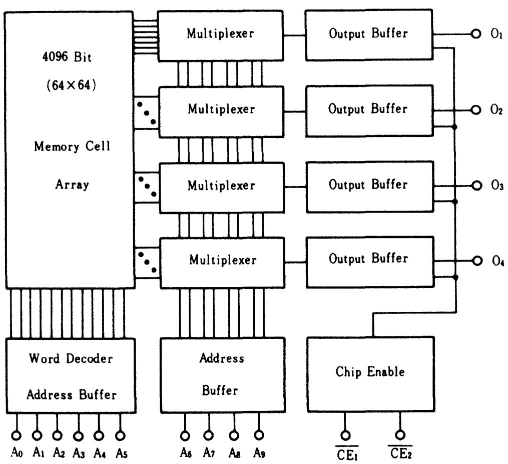


(DG-18)

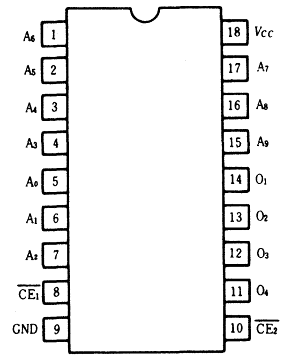
■ FEATURES

- 1024 words x 4 bits organization (fully decoded)
- DTL/TTL Compatible inputs and outputs
- Fast read access time; 30 ns typ. (50 ns max.)
- Medium power consumption; 500 mW typ.
- Two Chip enable inputs for memory expansion
- Open collector outputs (HN25044)/Three-state outputs (HN25045)
- Standard cerdip 18-pin package

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS ($Ta=25°C$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{out}	50	mA
Operating Temperature	T_{opr}	−25 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

■ DC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to +75°C)

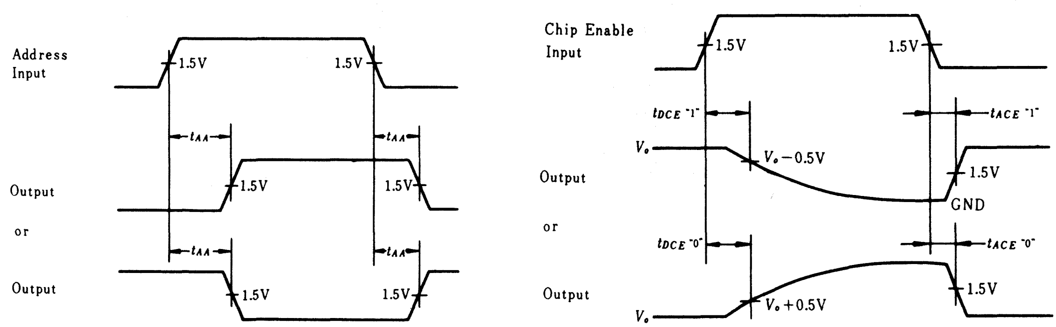
Item	Symbol	Test Condition	HN25044			HN25045			Unit
			min	typ	max	min	typ	max	
Input Voltage	V_{IH}		2.0	—	—	2.0	—	—	V
	V_{IL}		—	—	0.8	—	—	0.8	V
Output Voltage	V_{OH}	I_{OH}=−2mA	—	—	—	2.4	—	—	V
	V_{OL}	I_{OL}=16mA	—	—	0.45	—	—	0.45	V
Input Current	I_{IH}	V_{IH}=2.7V	—	—	40	—	—	40	μA
	I_{IL}	V_{IL}=0.4V	—	—	−0.4	—	—	−0.4	mA
Output Leakage Current	I_{OLK}	V_{out}=5.5V	—	—	100	—	—	100	μA
		V_{out}=0.4V	—	—	40	—	—	40	
Input Clamp Voltage	V_I	I_{in}=−18mA	—	—	−1.2	—	—	−1.2	V
Power Supply Current	I_{CC}	Input Either Open or at Ground	—	100	130	—	100	130	mA
Output Short-circuit Current	I_{OS}	V_{out}=0V	—	—	—	15	30	60	mA
Input Capacitance	C_{in}	V_{in}=2V, V_{CC}=0V	—	5	10	—	5	10	pF
Output Capacitance	C_{out}	V_{out}=0V, V_{CC}=0V	—	7	12	—	7	12	pF

■ AC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to 75°C)

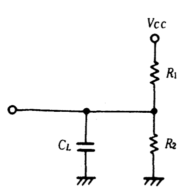
Item	Symbol	min	typ	max	Unit
Address Access Time	t_{AA}	—	35	50	ns
Chip Enable Access Time	t_{ACE}	—	20	30	ns
Chip Enable Disable Time	t_{DCE}	—	20	30	ns

Notes: 1. Typ. value is at V_{CC}=5.0 V and T_a = 25°C
2. Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5 V from the active output level.

■ SWITCHING WAVEFORMS



■ SWITCHING TIME TEST CONDITIONS



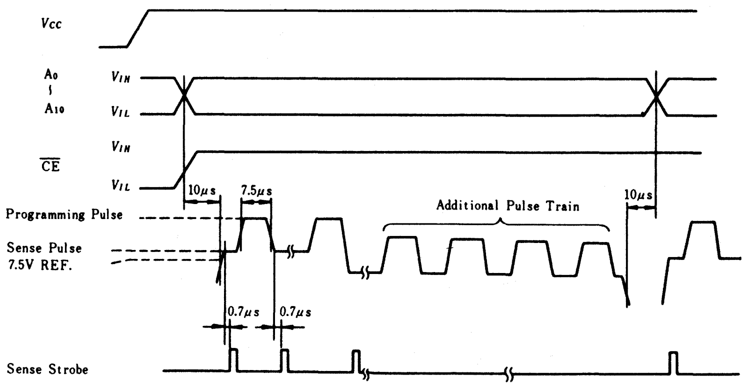
SWITCHING PARAMETER	HN25044			HN25045		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF	300Ω	600Ω	30pF
t_{ACE} "1"	—	—	—	∞	600Ω	10pF
t_{ACE} "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t_{DCE} "1"	—	—	—	∞	600Ω	30pF
t_{DCE} "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

INPUT CONDITIONS
Amplitude - 0V to 3V
Rise and Fall time - 5ns from 1V to 2V
Frequency - 1MHz

■PROGRAMMING SPECIFICATION

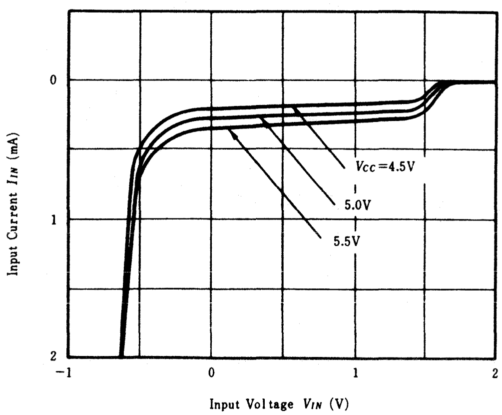
Characteristic	Limit	Unit	Notes
Ambient Temperature	25±5	°C	
Programming Pulse Amplitude Clamp Voltage Ramp Rate Pulse Width Duty Cycle	 130±5% 20+0% −2% 70max 7.5±5% 70% min	 mA V V/μs μs 	 10V point/150Ω load
Sense Current Amplitude Clamp Voltage Ramp Rate Sense current interruption before and after address change	 20±0.5 20+0% −2% 70max 10min	 mA V V/μs μs	 10V point/150Ω load
Programming V_{CC}	5.0+5% −0%	V	
Maximum Sensed Voltage for programmed "1"	7.5±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7min	μs	
Programming Time Allocation/Bit	100max	ms	
Additional Programming Pulse Number	4	Time	

■TYPICAL WAVEFORMS

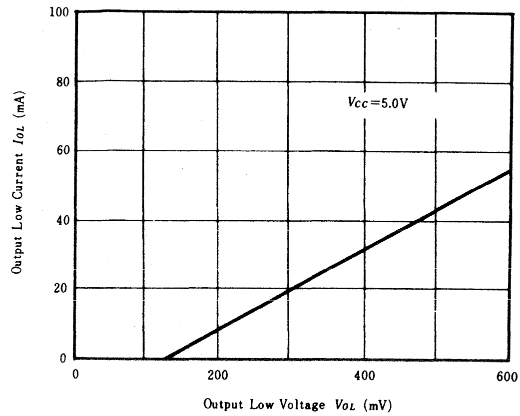


■ TYPICAL DC CHARACTERISTICS

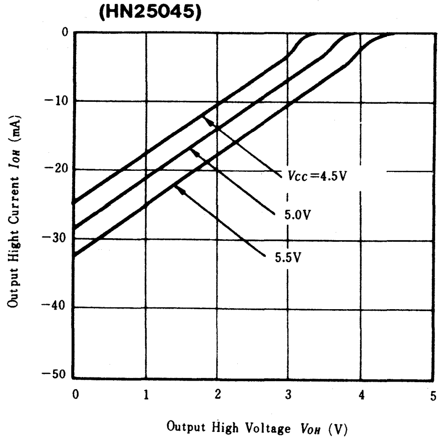
INPUT CURRENT vs. INPUT VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE

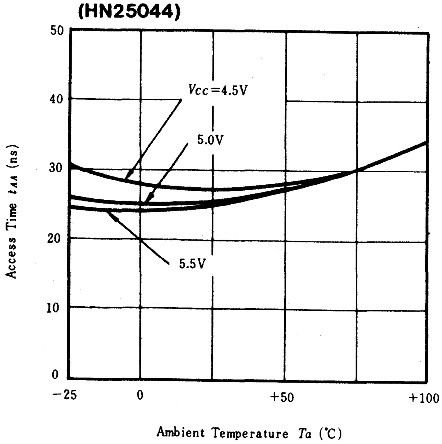


OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE (HN25045)

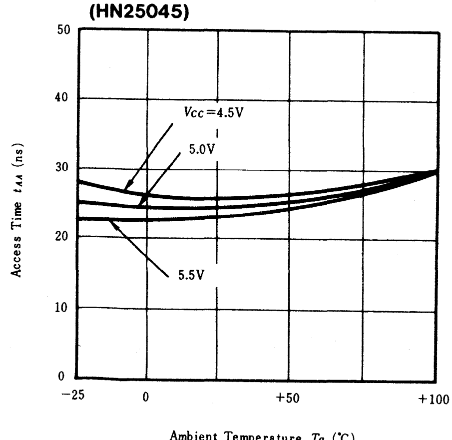


■ TYPICAL AC CHARACTERISTICS

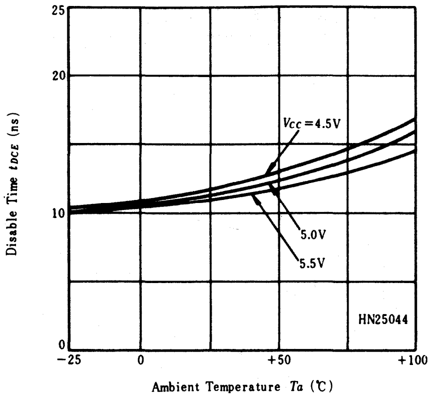
ACCESS TIME vs. AMBIENT TEMPERATURE (HN25044)



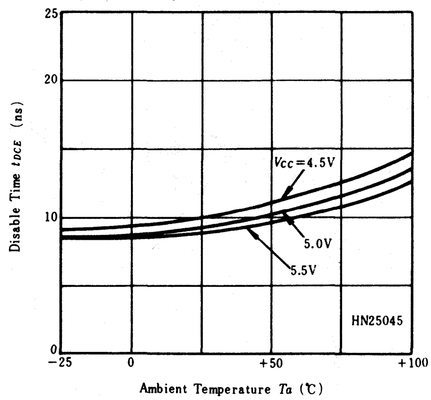
ACCESS TIME vs. AMBIENT TEMPERATURE (HN25045)



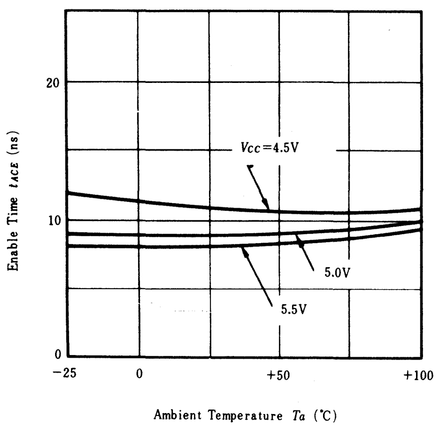
DISABLE TIME vs. AMBIENT TEMPERATURE (HN25044)



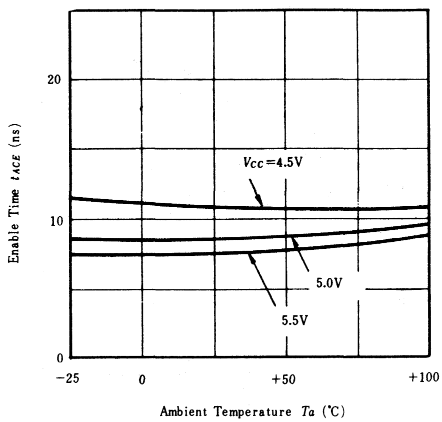
DISABLE TIME vs. AMBIENT TEMPERATURE (HN25045)



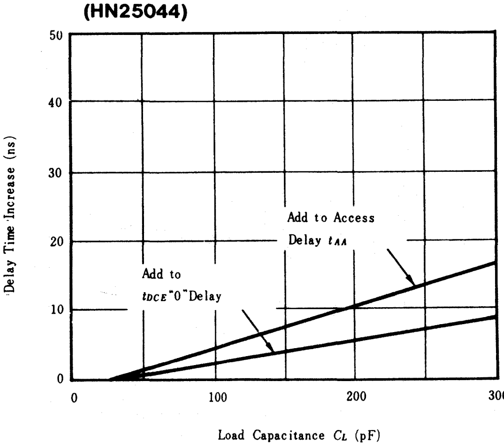
ENABLE TIME vs. AMBIENT TEMPERATURE (HN25044)



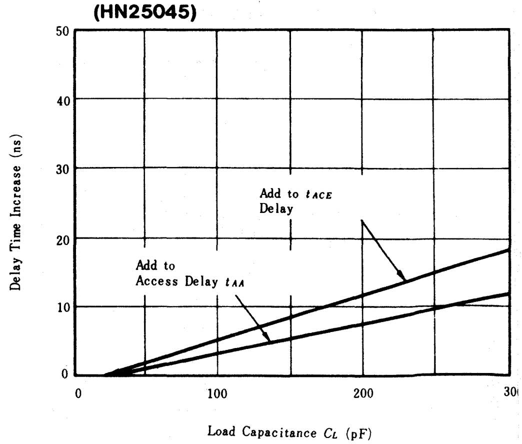
ENABLE TIME vs. AMBIENT TEMPERATURE (HN25045)



DELAY TIME INCREASE vs. LOAD CAPACITANCE (HN25044)



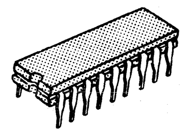
DELAY TIME INCREASE vs. LOAD CAPACITANCE (HN25045)



HN25084, HN25085

2048-word × 4-bit Programmable Read Only Memories

The HITACHI HN25084 and HN25085 are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 2048 word by 4 bit with on-chip address decoding and one chip enable input. The HN25084 and HN25085 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

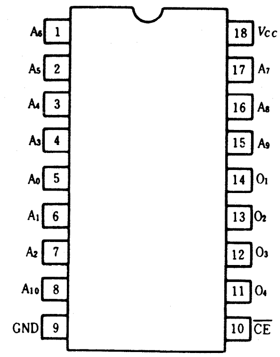


(DG-18)

■ FEATURES

- 2048 word x 4 bit organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 40 ns typ. (60 ns max)
- Medium power consumption: 550 mW typ.
- One chip enable input for memory expansion
- Open collector outputs (HN25084)/Three-state outputs (HN25085)
- Standard cerdip 18-pin dual in-line package

■ PIN ARRANGEMENT



(Top View)

■ OPERATION

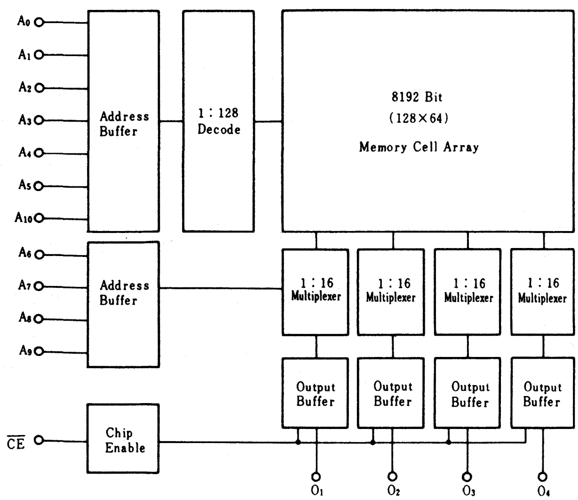
- **Programming**

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the eleven address inputs in TTL level. The device is disabled by bringing $\overline{CE}$ to a logic "one". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic "one" state, an additional pulse train is applied, then is stopped.

- **Reading**

To read the memory the device is enabled by bringing $\overline{CE}$ to a logic "zero". The outputs then correspond to the data programmed in the selected word.

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{out}	50	mA
Operating Temperature	T_{opr}	−25 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

■ DC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Input High Voltage	V_{IH}		2.0	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Input High Current	I_{IH}	V_I=2.7V	—	—	40	μA
Input Low Current	$-I_{IL}$	V_I=0.4V	—	—	0.40	mA
Output Low Voltage	V_{OL}	I_{OL}=16mA	—	—	0.45	V
Output Leakage Current	I_{OLK1}	V_O=5.25V	—	—	100	μA
Output Leakage Current	I_{OLK2}	V_O=0.4V	—	—	40	μA
Input Clamp Voltage	V_I	I_I=−18mA	—	—	−1.2	V
Power Supply Current	I_{CC}	Inputs Either Open or at Ground	—	110	150	mA
Output High Voltage*	V_{OH}	I_O=−2mA	2.4	—	—	V
Output Short Circuit Current*	$-I_{OS}$	V_O=0V	15	—	60	mA

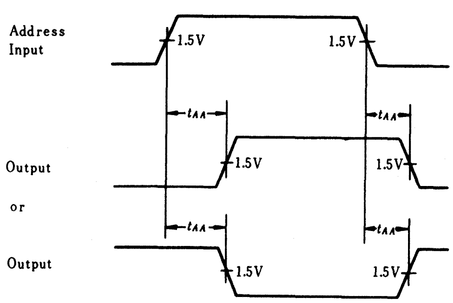
* Note: Applicable to HN25089 only.

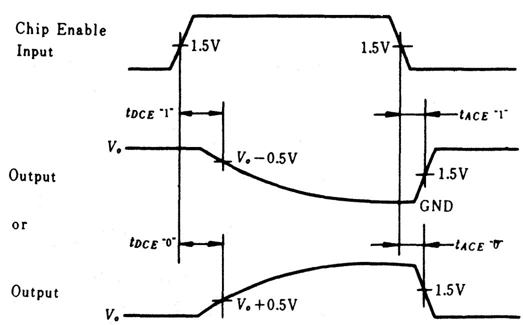
■ AC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	t_{AA}		—	40	60	ns
Chip Enable Access Time	t_{ACE}		—	20	35	ns
Chip Enable Disable Time	t_{DCE}		—	20	35	ns

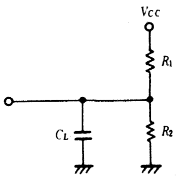
Note) 1. Output Load: See Test Circuit.
2. Measurement Reference: 1.5V for both inputs and outputs.

■ SWITCHING WAVEFORMS





SWITCHING TIME TEST CONDITIONS



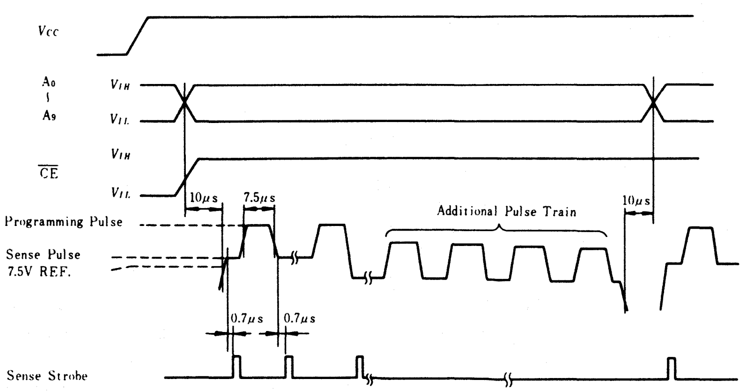
SWITCHING PARAMETER	HN25084			HN25085		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF	300Ω	600Ω	30pF
t_{ACE} "1"	—	—	—	∞	600Ω	10pF
t_{ACE} "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t_{DCE} "1"	—	—	—	∞	600Ω	30pF
t_{DCE} "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

INPUT CONDITIONS
Amplitude — 0V to 3V
Rise and Fall time — 5ns from 1V to 2V
Frequency — 1MHz

PROGRAMMING SPECIFICATION

Characteristic	Limit	Unit	Notes
Ambient Temperature	25±5	°C	
Programming Pulse Amplitude Clamp Voltage Ramp Rate Pulse Width Duty Cycle	 130±5% 20±2% 70max 7.5±5% 70% min	 mA V V/μs μs	 10V point/150Ω load
Sense Current Amplitude Clamp Voltage Ramp Rate Sense Current Interruption before and after address change	 20±0.5 20±2% 70max 10min	 mA V V/μs μs	
Programming V_{CC}	5.0+5% −0%	V	
Maximum Sensed Voltage for programmed "1"	7.5±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7min	μs	
Programming Pulse Number	100max	ms	
Additional Programming Pulse Number	4	Time	

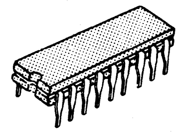
TYPICAL WAVEFORMS



HN25084S, HN25085S —— Preliminary

2048-word × 4-bit Programmable Read Only Memories

The HITACHI HN25084S and HN25085S are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 2048 words by 4 bits with on-chip address decoding and one chip enable input. The HN25084S and HN25085S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.



(DG-18)

■ FEATURES

- 2048 words x 4 bits organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 25 ns typ. (50 ns max)
- Medium power consumption: 550 mW typ.
- One chip enable input for memory expansion
- Open collector outputs (HN25084S)/Three-state outputs (HN25085S)
- Standard cerdip 18-pin dual in-line package

■ OPERATION

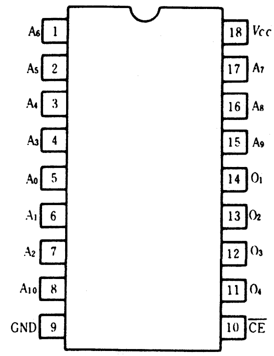
- **Programming**

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the eleven address inputs in TTL level. The device is disabled by bringing $\overline{CE}$ to a logic "one". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic "one" state, an additional pulse train is applied, then is stopped.

- **Reading**

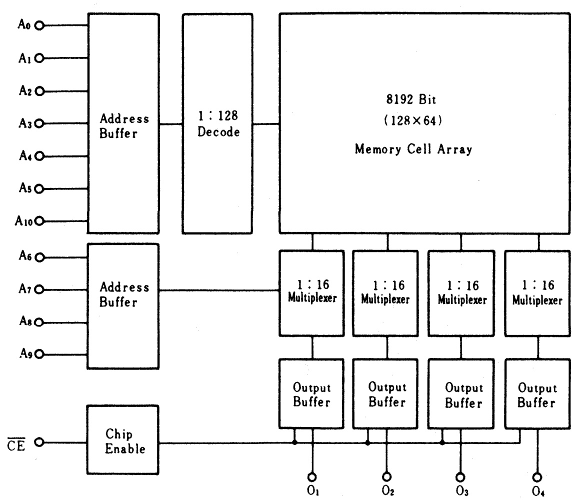
To read the memory the device is enabled by bringing $\overline{CE}$ to a logic "zero". The outputs then correspond to the data programmed in the selected word.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{out}	50	mA
Operating Temperature	T_{opr}	−25 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

■DC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Input High Voltage	V_{IH}		2.0	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Input High Current	I_{IH}	V_I=2.7V	—	—	40	μA
Input Low Current	$-I_{IL}$	V_I=0.4V	—	—	0.40	mA
Output Low Voltage	V_{OL}	I_O=16mA	—	—	0.45	V
Output Leakage Current	I_{OLK1}	V_O=5.25V	—	—	100	μA
Output Leakage Current	I_{OLK2}	V_O=0.4V	—	—	40	μA
Input Clamp Voltage	V_I	I_I=−18mA	—	—	−1.2	V
Power Supply Current	I_{CC}	Inputs Either Open or at Ground	—	110	160	mA
Output High Voltage*	V_{OH}	I_O=−2mA	2.4	—	—	V
Output Short Circuit Current*	$-I_{OS}$	V_O=0V	15	—	60	mA

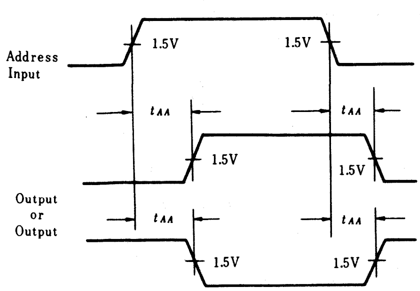
* Note: Applicable to HN25089 only.

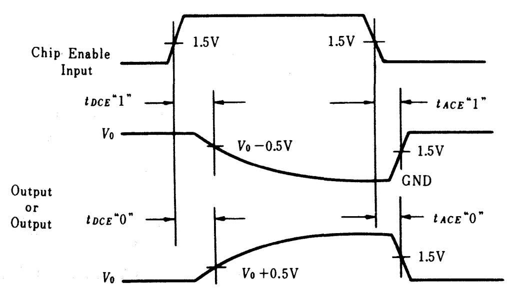
■AC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	t_{AA}		—	25	50	ns
Chip Enable Access Time	t_{ACE}		—	20	35	ns
Chip Enable Disable Time	t_{DCE}		—	15	35	ns

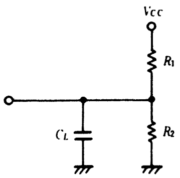
Note) 1. Output Load: See Test Circuit.
2. Measurement Reference: 1.5V for both inputs and outputs.

■SWITCHING WAVEFORMS





■ SWITCHING TIME TEST CONDITIONS

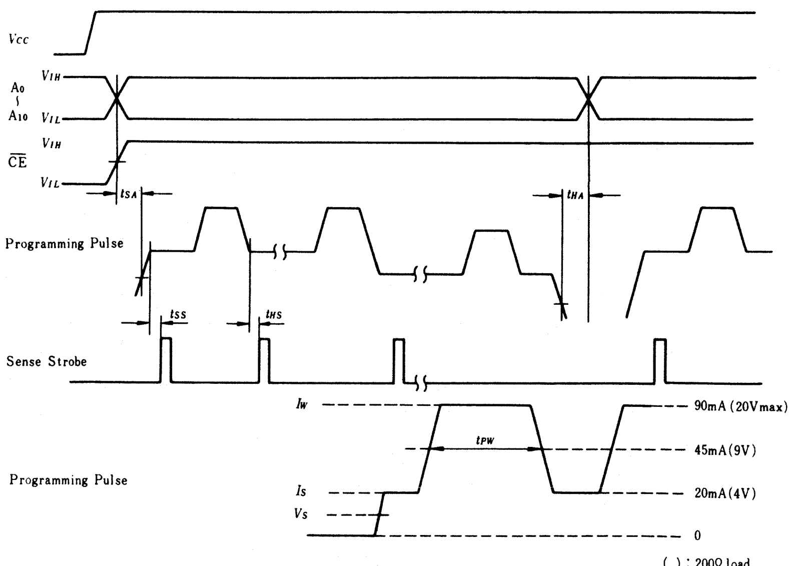


SWITCHING PARAMETER	HN25084S			HN25085S		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF	300Ω	600Ω	30pF
t_{ACE} "1"	—	—	—	∞	600Ω	10pF
t_{ACE} "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t_{DCE} "1"	—	—	—	∞	600Ω	30pF
t_{DCE} "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

INPUT CONDITIONS
Amplitude−0V to 3V
Rise and Fall time−5ns from 1V to 2V
Frequency−1MHz

■ PROGRAMING SPECIFICATION

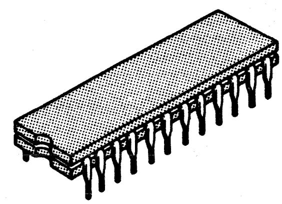
PARAMETER	Symbol	min	typ	max	Unit	Note
Ambient Temperature	Ta	20	25	30	°C	
Programming V_{CC}	V_{CC}	4.75	5.0	5.25	V	
Programming Pulse						
Amplitude	I_W	88	90	92	mA	
Clamp Voltage	V_W	19.0	19.5	20.0	V	
Ramp Rate		10	—	70	V/μs	
Pulse Width	t_{PW}	7.1	7.5	7.9	μs	9V point/200Ω load
Duty Cycle		70	—	—	%	
Sense Current						
Amplitude	I_S	19	20	21	mA	
Sense Voltage	V_S	7.4	7.5	7.6	V	
Clamp Voltage		19.0	19.5	20.0	V	
Ramp Rate		70	—	—	V/μs	
Address Setup Time	t_{SA}	10	—	—	μs	
Address Hold Time	t_{HA}	10	—	—	μs	
Sense Setup Time	t_{SS}	0.7	—	—	μs	
Sense Hold Time	t_{HS}	0.7	—	—	μs	
Additional Programming Pulse		1	1	1	time	
Programming Pulse Number per bit	n	—	—	10000	time	



HN25088, HN25089

1024-word × 8-bit Programmable Read Only Memories

The HITACHI HN25088 and HN25089 are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 1024 words by 8 bits with on-chip address decoding and four chip enable inputs. The HN25088 and HN25089 are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

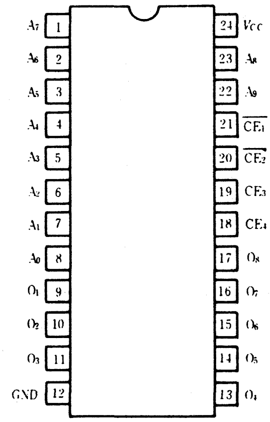


(DG-24)

■ FEATURES

- 1024 words x 8 bits organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 40 ns (typ), 60 ns (max)
- Medium power consumption: 600 mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088)/Three-state outputs (HN25089)
- Standard cerdip 24-pin dual in-line package

■ PIN ARRANGEMENT



(Top View)

■ OPERATION

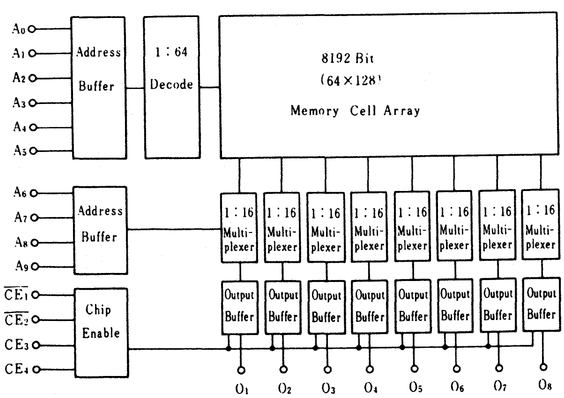
- **Programming**

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing $\overline{CE1}$ and/or $\overline{CE2}$ to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

- **Reading**

To read the memory the device is enabled by bringing $\overline{CE1}$ and $\overline{CE2}$ to a logic "zero". CE3 and CE4 to a logic "one". The outputs them corresponed to the data programmed in the selected word.

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{out}	50	mA
Operating Temperature	T_{opr}	−25 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

■ DC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to +75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Input High Voltage	V_{IH}		2.0	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Input High Current	I_{IH}	V_I=2.7V	—	—	40	μA
Input Low Current	$-I_{IL}$	V_I=0.4V	—	—	0.40	mA
Output Low Voltage	V_{OL}	I_{OL}=16mA	—	—	0.45	V
Output Leakage Current	I_{OLK1}	V_O=5.25V	—	—	100	μA
Output Leakage Current	I_{OLK2}	V_O=0.4V	—	—	40	μA
Input Clamp Voltage	V_I	I_I=−18mA	—	—	−1.2	V
Power Supply Current	I_{CC}	Inputs Either Open or at Ground	—	120	160	mA
Output High Voltage*	V_{OH}	I_{OH}=−2mA	2.4	—	—	V
Output Short Circuit Current*	$-I_{OS}$	V_O=0V	15	—	60	mA

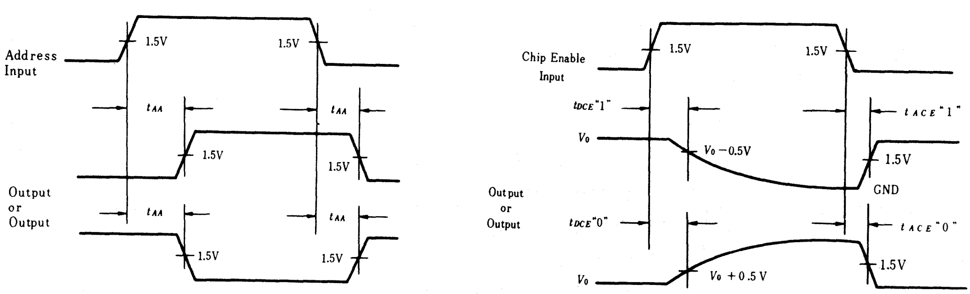
* Note: Applicable to HN25089 only.

■ AC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to 75°C)

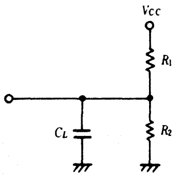
Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	t_{AA}		—	40	60	ns
Chip Enable Access Time	t_{ACE}		—	20	35	ns
Chip Enable Disable Time	t_{DCE}		—	20	35	ns

Note) 1. Output Load: See Test Circuit.
2. Measurement Reference: 1.5V for both inputs and outputs.

■ SWITCHING WAVEFORMS



■ SWITCHING TIME TEST CONDITIONS

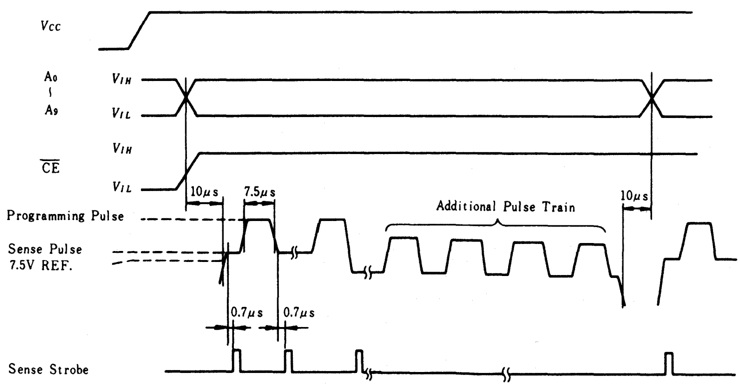


SWITCHING PARAMETER	HN25088			HN25089		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF	300Ω	600Ω	30pF
t_{ACE} "1"	—	—	—	∞	600Ω	10pF
t_{ACE} "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t_{DCE} "1"	—	—	—	∞	600Ω	30pF
t_{DCE} "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

INPUT CONDITIONS
Amplitude – 0V to 3V
Rise and Fall time – 5ns from 1V to 2V
Frequency – 1MHz

■ PROGRAMMING SPECIFICATION

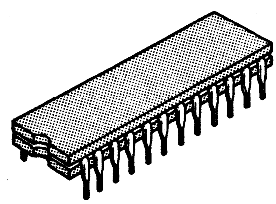
Characteristic	Limit	Unit	Notes
Ambient Temperature	25±5	°C	
Programming Pulse			
Amplitude	130±5%	mA	
Clamp Voltage	20±2%	V	
Ramp Rate	70max	V/μs	
Pulse Width	7.5±5%	μs	10V point/150Ω load
Duty Cycle	70% min		
Sense Current			
Amplitude	20±0.5	mA	
Clamp Voltage	20±2%	V	
Ramp Rate	70max	V/μs	
Sense Current Interruption before and after address change	10min	μs	
Programming V_{CC}	5.0+5% −0%	V	
Maximum Sensed Voltage for programmed "1"	7.5±0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7min	μs	
Programming Pulse Number	100max	ms	
Additional Programming Pulse Number	4	Time	



HN25088S, HN25089S —— Preliminary

1024-word × 8-bit Programmable Read Only Memories

The HITACHI HN25088S and HN25089S are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit-read only memories organized as 1024 words by 8 bits with on-chip address decoding and four chip enable inputs. The HN25088S and HN25089S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

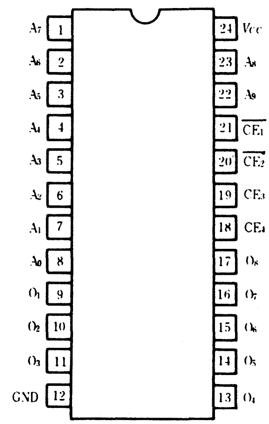


(DG-24)

■ FEATURES

- 1024 words x 8 bits organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 25 ns typ. (50 ns max)
- Medium power consumption: 600 mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088S)/Three-state outputs (HN25089S)
- Standard cerdip 24-pin dual in-line package

■ PIN ARRANGEMENT



(Top View)

■ OPERATION

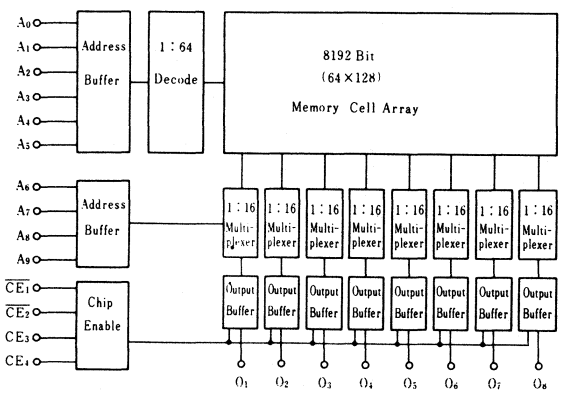
- **Programming**

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing $\overline{CE1}$ and/or $\overline{CE2}$ to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

- **Reading**

To read the memory the device is enabled by bringing $\overline{CE1}$ and $\overline{CE2}$ to a logic "zero", CE3 and CE4 to a logic "one". The outputs then corresponed to the data programmed in the selected word.

■ LOGIC DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{out}	50	mA
Operating Temperature	T_{opr}	−25 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

■ DC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to +75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Input High Voltage	V_{IH}		2.0	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Input High Current	I_{IH}	V_I=2.7V	—	—	40	μA
Input Low Current	$-I_{IL}$	V_I=0.4V	—	—	0.40	mA
Output Low Voltage	V_{OL}	I_{OL}=16mA	—	—	0.45	V
Output Leakage Current	I_{OLK1}	V_O=5.25V	—	—	100	μA
Output Leakage Current	I_{OLK2}	V_O=0.4V	—	—	40	μA
Input Clamp Voltage	V_I	I_I=−18mA	—	—	−1.2	V
Power Supply Current	I_{CC}	Inputs Either Open or at Ground	—	120	160	mA
Output High Voltage*	V_{OH}	I_{OH}=−2mA	2.4	—	—	V
Output Short Circuit Current*	$-I_{OS}$	V_O=0V	15	—	60	mA

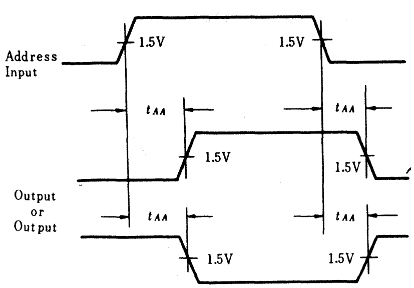
* Note: Applicable to HN25089S only.

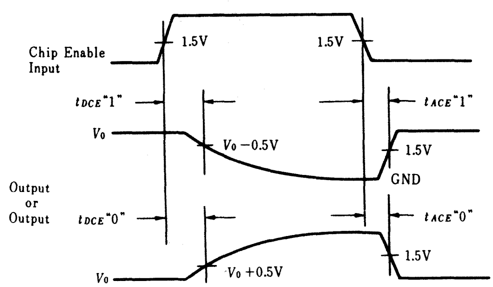
■ AC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	t_{AA}		—	25	50	ns
Chip Enable Access Time	t_{ACE}		—	20	35	ns
Chip Enable Disable Time	t_{DCE}		—	15	35	ns

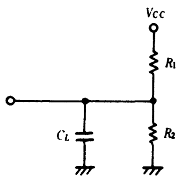
Note) 1. Output Load: See Test Circuit.
2. Measurement Reference: 1.5V for both inputs and outputs.

■ SWITCHING WAVEFORMS





■ SWITCHING TIME TEST CONDITIONS

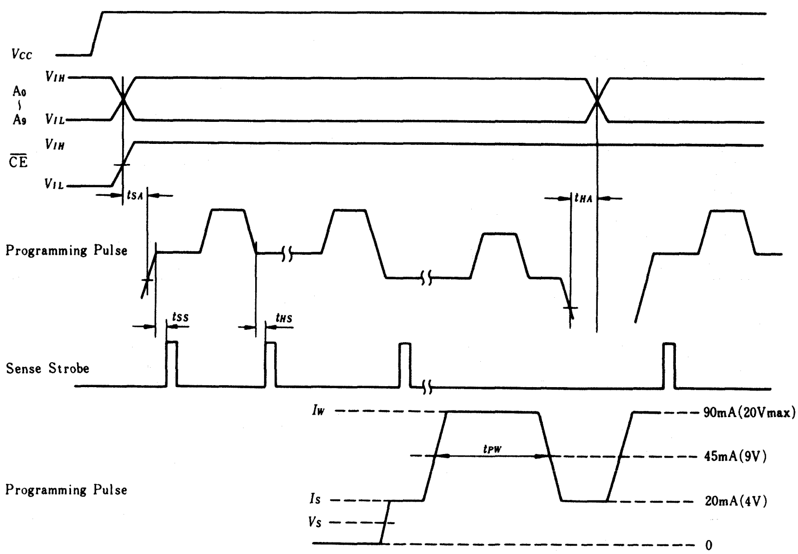


SWITCHING PARAMETER	HN25088S			HN25089S		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF	300Ω	600Ω	30pF
t_{ACE} "1"	—	—	—	∞	600Ω	10pF
t_{ACE} "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t_{DCE} "1"	—	—	—	∞	600Ω	30pF
t_{DCE} "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

INPUT CONDITIONS
Amplitude — 0V to 3V
Rise and Fall time — 5ns from 1V to 2V
Frequency — 1MHz

■ PROGRAMING SPECIFICATION

PARAMETER	Symbol	min	typ	max	Unit	Note
Ambient Temperature	Ta	20	25	30	°C	
Programming V_{CC}	V_{CC}	4.75	5.0	5.25	V	
Programming Pulse						
Amplitude	I_W	88	90	92	mA	
Clamp Voltage	V_W	19.0	19.5	20.0	V	
Ramp Rate		10	—	70	V/μs	
Pulse Width	t_{PW}	7.1	7.5	7.9	μs	9V point/200Ω load
Duty Cycle		70	—	—	%	
Sense Current						
Amplitude	I_S	19	20	21	mA	
Sense Voltage	V_S	7.4	7.5	7.6	V	
Clamp Voltage		19.0	19.5	20.0	V	
Ramp Rate		70	—	—	V/μs	
Address Setup Time	t_{SA}	10	—	—	μs	
Address Hold Time	t_{HA}	10	—	—	μs	
Sense Setup Time	t_{SS}	0.7	—	—	μs	
Sense Hold Time	t_{HS}	0.7	—	—	μs	
Additional Programming Pulse		1	1	1	time	
Programming Pulse Number per bit	n	—	—	10000	time	



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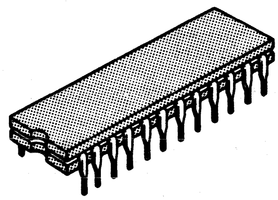
HN25168S, HN25169S ——— Preliminary

2048-word × 8-bit Programmable Read Only Memories

The HITACHI HN25168S and HN25169S are high speed electrically programmable, fully decoded TTL Bipolar 16384 bit read only memories organized as 2048 words by 8 bits with on-chip address decoding and three chip enable inputs. The HN25168S and HN25166S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

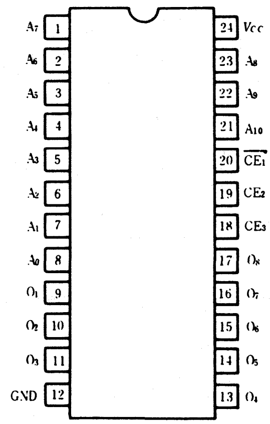


(DG-24)

■ FEATURES

- 2048 words x 8 bits organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 40 ns typ. (60 ns max)
- Medium power consumption: 600 mW typ.
- Three chip enable inputs for memory expansion.
- Open collector outputs (HN25168S)/Three-state outputs (HN25169S)
- Standard cerdip 24-pin dual in-line package

■ PIN ARRANGEMENT



(Top View)

■ OPERATION

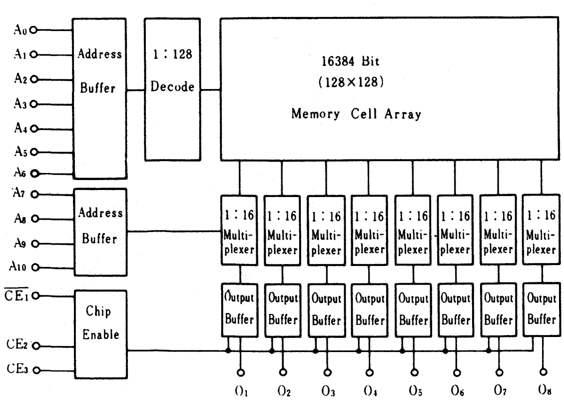
- **Programming**

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired world is selected by the eleven address inputs in TTL level. The device is disabled by bringing $\overline{CE1}$ to as logic "one" or CE2 and/or CE3 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse is applied, then is stopped.

- **Reading**

To read the memory the device is enabled by bringing $\overline{CE1}$ to a logic "zero", CE2 and CE3 to a logic "one". The outputs then corresponed to the data programmed in the selected word.

■ LOGIC DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +5.5	V
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{out}	50	mA
Operating Temperature	T_{opr}	−25 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

■ DC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to +75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Input High Voltage	V_{IH}		2.0	—	—	V
Input Low Voltage	V_{IL}		—	—	0.8	V
Input High Current	I_{IH}	V_I=2.7V	—	—	40	μA
Input Low Current	$-I_{IL}$	V_I=0.4V	—	—	0.40	mA
Output Low Voltage	V_{OL}	I_{OL}=16mA	—	—	0.45	V
Output Leakage Current	I_{OLK1}	V_O=5.25V	—	—	100	μA
Output Leakage Current	I_{OLK2}	V_O=0.4V	—	—	40	μA
Input Clamp Voltage	V_I	I_I=−18mA	—	—	−1.2	V
Power Supply Current	I_{CC}	Inputs Either Open or at Ground	—	120	170	mA
Output High Voltage*	V_{OH}	I_{OH}=−2mA	2.4	—	—	V
Output Short Circuit Current*	$-I_{OS}$	V_O=0V	15	—	60	mA

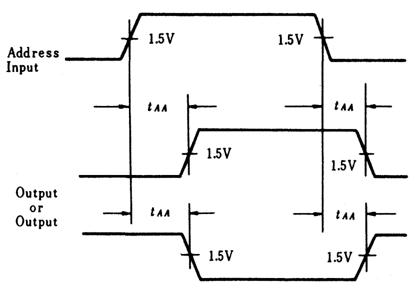
* Note: Applicable to HN25169S only.

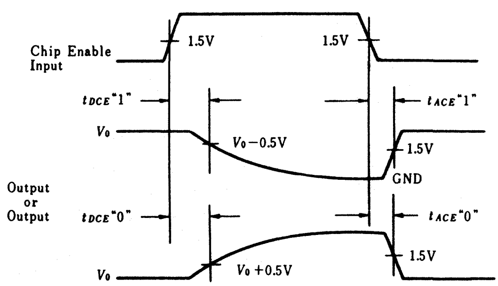
■ AC CHARACTERISTICS (V_{CC}=4.75 to 5.25V, Ta=0 to 75°C)

Characteristic	Symbol	Test Conditions	min	typ	max	Unit
Address Access Time	t_{AA}		—	40	60	ns
Chip Enable Access Time	t_{ACE}		—	20	35	ns
Chip Enable Disable Time	t_{DCE}		—	20	35	ns

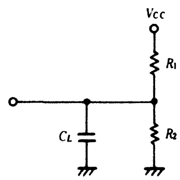
Note) 1. Output Load: See Test Circuit.
2. Measurement Reference: 1.5V for both inputs and outputs.

■ SWITCHING WAVEFORMS





■SWITCHING TIME TEST CONDITIONS

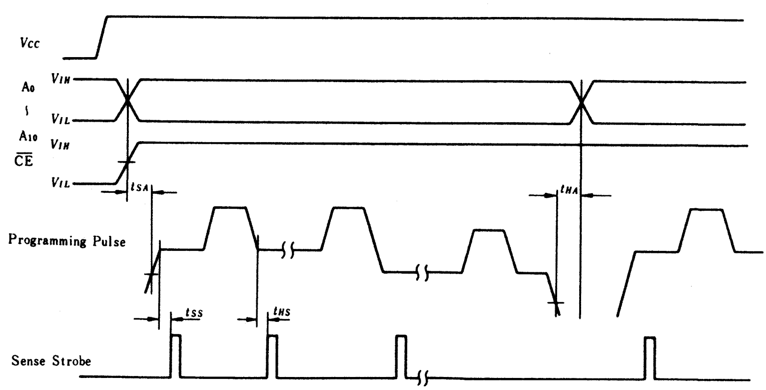


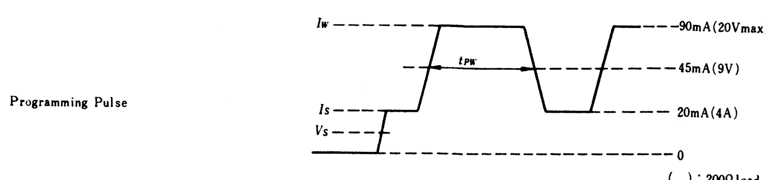
SWITCHING PARAMETER	HN25168S			HN25169S		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF	300Ω	600Ω	30pF
t_{ACE} "1"	—	—	—	∞	600Ω	10pF
t_{ACE} "0"	300Ω	600Ω	10pF	300Ω	600Ω	10pF
t_{DCE} "1"	—	—	—	∞	600Ω	30pF
t_{DCE} "0"	300Ω	600Ω	30pF	300Ω	600Ω	30pF

INPUT CONDITIONS
Amplitude − 0V to 3V
Rise and Fall time − 5ns from 1V to 2V
Frequency − 1MHz

■PROGRAMING SPECIFICATION

PARAMETER	Symbol	min	typ	max	Unit	Note
Ambient Temperature	Ta	20	25	30	°C	
Programming V_{CC}	V_{CC}	4.75	5.0	5.25	V	
Programming Pulse						
Amplitude	I_W	88	90	92	mA	
Clamp Voltage	V_W	19.0	19.5	20.0	V	
Ramp Rate		10	—	70	V/μs	
Pulse Width	t_{PW}	7.1	7.5	7.9	μs	9V point/200Ω load
Duty Cycle		70	—	—	%	
Sense Current						
Amplitude	I_S	19	20	21	mA	
Sense Voltage	V_S	7.4	7.5	7.6	V	
Clamp Voltage		19.0	19.5	20.0	V	
Ramp Rate		70	—	—	V/μs	
Address Setup Time	t_{SA}	10	—	—	μs	
Address Hold Time	t_{HA}	10	—	—	μs	
Sense Setup Time	t_{SS}	0.7	—	—	μs	
Sense Hold Time	t_{HS}	0.7	—	—	μs	
Additional Programming Pulse		1	1	1	time	
Programming Pulse Number per bit	n	—	—	10000	time	





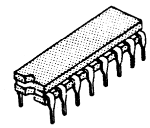
MEMORY SUPPORT CIRCUITS

HD2912

Quadruple TTL-to-MOS Clock Drivers

The HD2912, a clock driver for the MOS memory, has basically the NAND function. Its input is a TTL level and its output becomes and N MOS clock input level. It operates on two power supplies – V_{CC} (5V) and V_{DD} (12V). It anticipates taking as its load a maximum of ten units of 4K-bit N MOS memories and can drive a load capacity of 400 pF at high speed.

- TTL-MOS level converter circuit
- Switching time: 50 ns (max.)
- Load capacity drivable: 600pF
- Mounted with 4 circuits
- Applicable temperature: 0 to 70°C



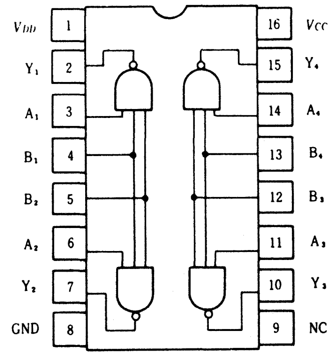
(DG-16)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HD2912	Unit
Supply Voltage	V_{CC}*	7.0	V
	V_{DD}*	18.0	V
Input Voltage	V_{in}*	5.5	V
Load Capacitance	C_L**	600	pF
Power Dissipation	P_T***	800	mW
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* With respect GND
** per circuit
*** per package

■ PIN ARRANGEMENT



(Top View)

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{DD}	11.4	12	12.6	V
Operating Temperature	T_{opr}	0	25	70	°C
Load Capacitance	C_L	100	—	600	pF
Damping Resistance	R_D	10	—	—	Ω

■ ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V ±5%, V_{DD}=12V ±5%)

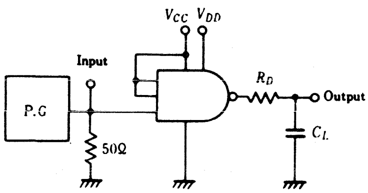
Item		Symbol	Test Condition	min	typ*	max	Unit
Input Voltage		V_{IL}		2.0	—	—	V
		V_{IH}		—	—	0.8	V
Output Voltage		V_{OL}	V_{in}=2V, I_{OL}=0.1mA	—	0.45	0.6	V
		V_{OH}	V_{in}=0.8V, I_{OH}=−0.1mA	V_{DD}−0.9	11.5	—	V
Input Current	A	I_{IL}	V_{in}=0.4V	—	−1	−1.6	mA
	B	I_{IL}		—	−2	−3.2	mA
	A	I_{IH}	V_{in}=2.4V	—	—	40	μA
	B	I_{IH}		—	—	80	μA
		I_I	V_{in}=5.5V	—	—	1	mA
Power Supply Current		I_{DDH}	V_{in}=0V	—	16	24	mA
		I_{DDL}	V_{in}=5V	—	—	0.5	mA
		I_{CCH}	V_{in}=0V	—	12	18	mA
		I_{CCL}	V_{in}=5V	—	67	100	mA
Input Clamp Voltage		V_I	I_{in}=−12mA	—	—	−1.5	V

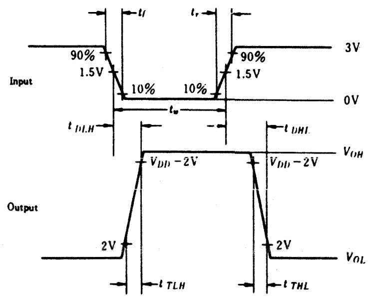
* V_{CC}=5V, V_{DD}=12V

■ SWITCHING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V, V_{DD}=12V)

Item	Symbol	Test Condition	min	typ	max	Unit
Rising Delay Time	t_{DLH}		—	35	50	ns
Falling Delay Time	t_{DHL}	C_L=300pF	—	25	45	ns
Rise Time	t_{TLH}	R_D=0Ω	—	12	25	ns
Fall Time	t_{THL}		—	12	25	ns

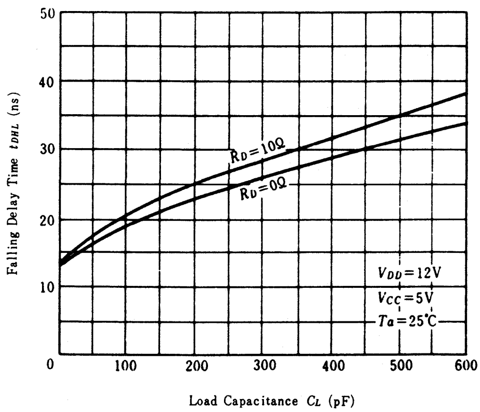
● TEST CIRCUIT AND WAVEFORMS



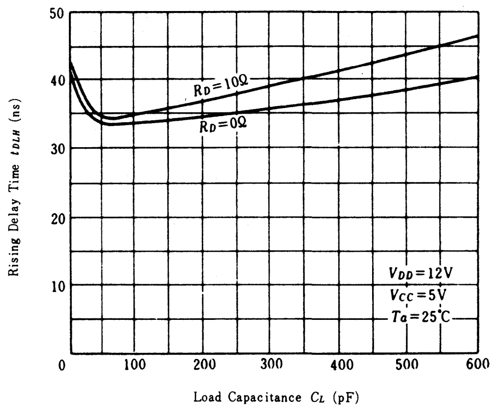


t_w=250ns, t_{cycle}=350ns, t_f = t_r = 10±1ns

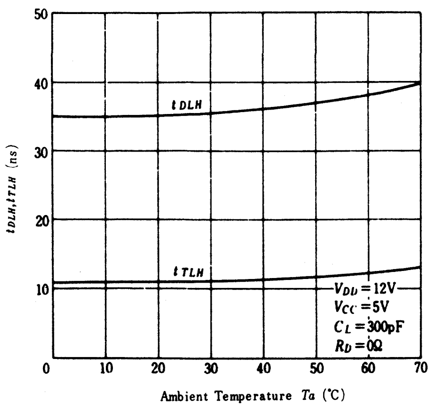
FALLING DELAY TIME vs. LOAD CAPACITANCE (1)



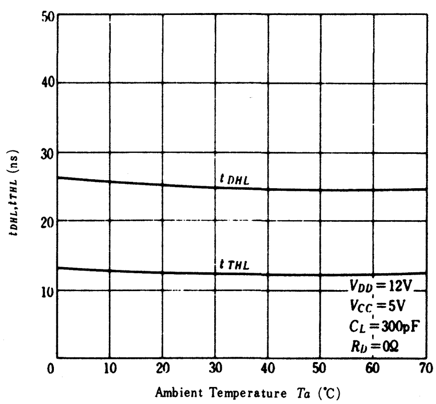
RISING DELAY TIME vs. LOAD CAPACITANCE (2)



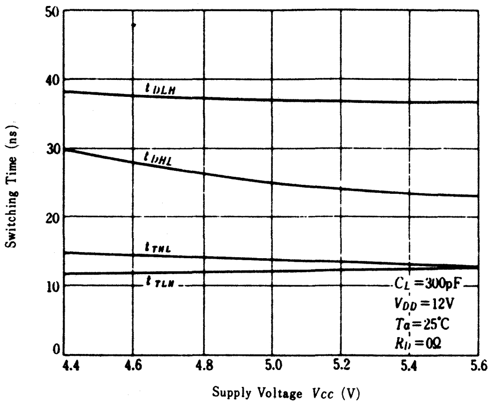
RISE TIME AND RISING DELAY TIME vs. AMBIENT TEMPERATURE



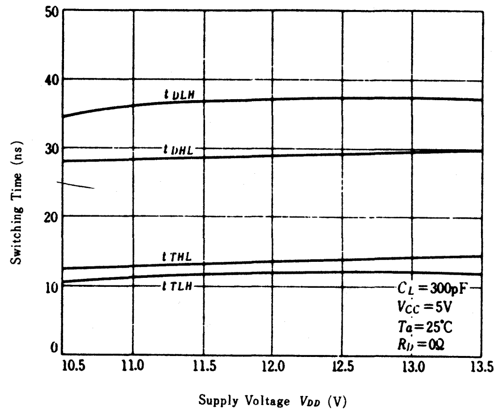
FALL TIME AND FALLING DELAY TIME vs. AMBIENT TEMPERATURE



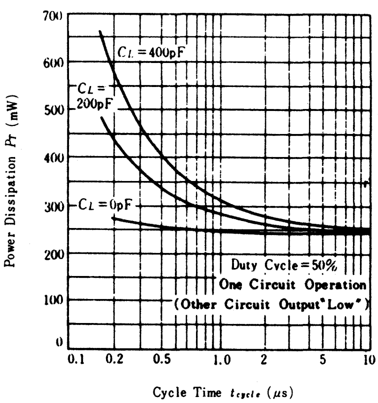
SWITCHING TIME vs. SUPPLY VOLTAGE (1)



SWITCHING TIME vs. SUPPLY VOLTAGE (2)



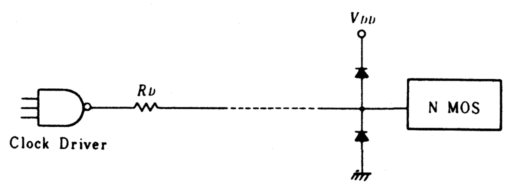
POWER DISSIPATION vs. CYCLE TIME



■ ITEMS REQUIRING CARE WHEN USING THE HD2912

When measuring or mounting the HD2912, consider the following.

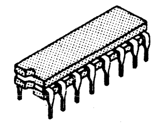
1. At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will breakdown.
2. When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may breakdown.
3. If its load capacity is less than a certainalue (100pF), sometimes this element cannot fully provide its function. Take note of this fact when designing a system.
4. When mounting this element, it is recommended providing the output terminal with a damping resistor (R_D) or a diode terminating circuit.



HD2916

Quadruple TTL-to-NMOS Clock Drivers

The HD2916, a clock driver for the MOS memory, basically possesses a NAND function. Its Input is a TTL level and its output becomes N MOS clock input level. It operates on two power supplies – V_{CC} (5V) and V_{DD} (12V). Assuming that a maximum of five units of 4K-bit N MOS memories may be connected, it is designed to drive a load capacity of 200pF at high speeds.

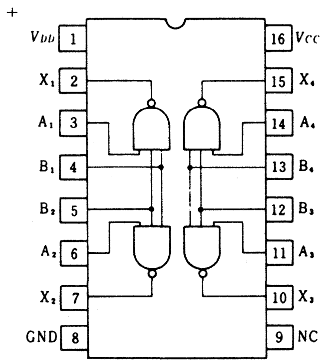


(DG-16A)

■ FEATURES

- TTL-MOS level converter
- Switching time: 50 ns (max.)
- Average power consumption: 600mW (max.)
- Load capacity drivable: 300pF
- Mounted with 4 circuits
- Applicable temperature: 10 to 65°C

■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HD2916	Unit
Supply Voltage	V_{CC}*	−0.5 to +7	V
	V_{DD}*	−0.5 to +15	V
Input Terminal Voltage	V_{IN}*	−0.5 to +5.5	V
Output Load Capacitance	C_L**	300	pF
Power Dissipation	P_T***	700	mW
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−50 to +150	°C

* With respect to GND
** Per circuit
*** Per package

■ RECOMMENDED OPERATING CONDITION

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{DD}	11.4	12.0	12.6	V
Operating Temperature	T_{opr}	10	25	55	°C
Input Voltage Level	V_{IH}	2.0	—	5.5	V
	V_{IL}	−0.5	—	0.8	V

■ ELECTRICAL CHARACTERISTICS (Ta=10 to 55°C, V_{CC}=5V ±5%, V_{DD}=12V ±5%)

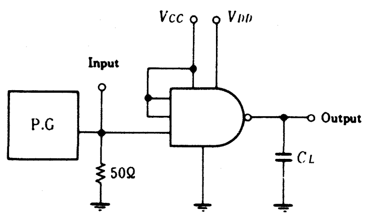
Item		Symbol	Test Condition	min	typ*	max	Unit
Input Current	A	I_{IH}	V_{IN}=2.4V	—	—	40	μA
		I_{IL}	V_{IN}=0.4V	—	−1	−2	mA
	B	I_{IH}	V_{IN}=2.4V	—	—	80	μA
		I_{IL}	V_{IN}=0.4V	—	−2	−4	mA
Output Voltage		V_{OH}	V_{IN}=0.8V, I_{OH}=−50μA	V_{DD}−0.7	V_{DD}−0.4	—	V
		V_{OL}	V_{IN}=2.0V, I_{OL}=50μA	—	0.3	0.45	V
Supply Current		I_{DDH}	V_{IN}=0V	—	13	20	mA
		I_{CCH}	V_{IN}=0V	—	13	40	mA
		I_{DDL}	V_{IN}=5V	—	—	39	mA
		I_{CCL}	V_{IN}=5V	—	40	60	mA
Average Power Dissipation		P_{TA}	C_L=300pF, f=1MHz t_w=0.5μs, one circuit operation	—	300	600	mW

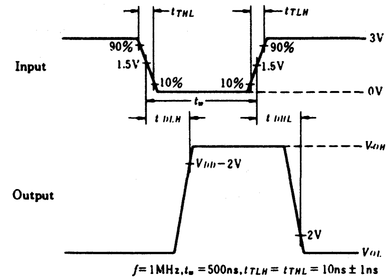
* V_{CC}=5V, V_{DD}=12V

■ SWITCHING CHARACTERISTICS (Ta=10 to 55°C, V_{CC}=5V ±5%, V_{DD}=12V ±5%)

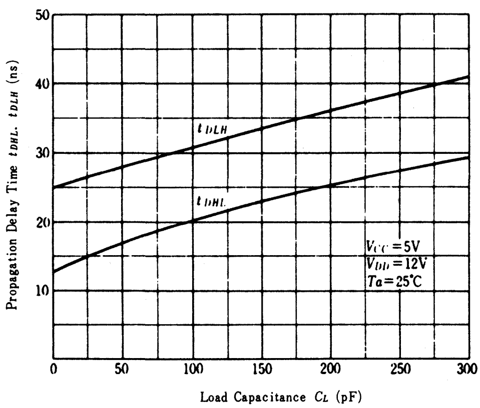
Item	Symbol	Test Condition	min	typ	max	Unit
Output Delay Time	t_{DLH}	C_L=200pF, f=1MHz, t_w=0.5μs	—	—	50	ns
	t_{DHL}		—	—	50	ns

● TEST CIRCUIT & WAVEFORMS

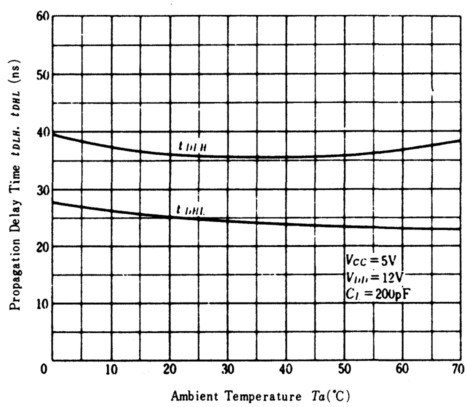




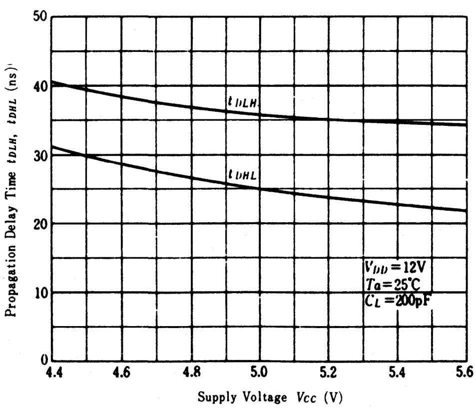
PROPAGATION DELAY TIME vs. LOAD CAPACITANCE



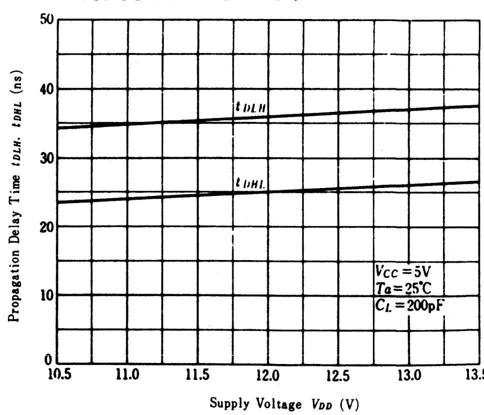
PROPAGATION DELAY TIME vs. AMBIENT TEMPERATURE



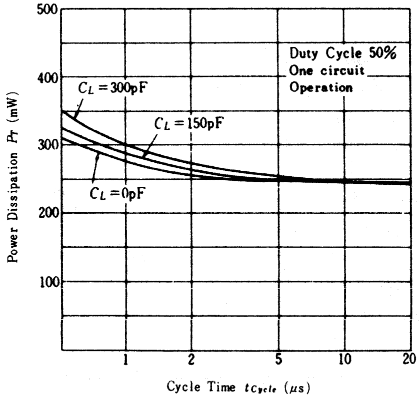
PROPAGATION DELAY TIME vs. SUPPLY VOLTAGE



PROPAGATION DELAY TIME vs. SUPPLY VOLTAGE



POWER DISSIPATION vs. CYCLE TIME



■ ITEMS REQUIRING CARE WHEN USING THE HD2916

When measuring or mounting the HD2916, consider the following:

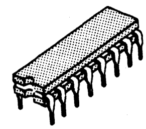
1. At the time of "H" level output, if a short circuit occurs between the output terminal and the other terminal (the GND terminal or input terminal), the element will breakdown.
2. When measuring the input/output characteristic of the circuit, do not place the input level in the vicinity of the threshold voltage (about 1.5V) for more than 10 seconds. If this caution is neglected, the element may breakdown.

HD2923

Quadruple ECL to TTL Drivers

The HD2923 is a monolithic, high speed Quadruple ECL to TTL Driver which accepts ECL input signals. It provides high output current suitable for driving the TTL clock inputs or other address multiplexing inputs of N-channel MOS memories such as the HM4816A of MK4116.Power supply requirements are ground, +5.0 Volts and −5.2 Volts. The HD2923 requires no particular power supply sequencing in order to assure standby mode of memories, because the outputs are always "high" at applying the power. Propagation delay is 10ns MAX.

The HD2923 is fabricated by means of HITACHI's Schottky Bipolar technology to assure high pert...nance over the 0°C to 75°C ambient temperature range.



(DG-16A)

■ FEATURES

- High Speed .... t_{pd} = 10ns MAX. (50% to 2.2V dc out or to +1.0V dc out, 200pF Load)
- Low Power .... 250mW typ. (DC)
- 10K ECL Compatible Inputs
- Pin Compatibility .... MC10125 or HD10125

■ ABSOLUTE MAXIMUM RATINGS

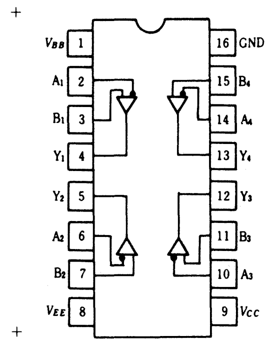
Item	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
	V_{EE}	−7 to +0.5	V
Input Voltage	V_{in}	V_{EE} to +0.5	V
Output Voltage	V_{out}	−1.0 to V_{CC}+1	V
Power Dissipation	P_T	1.0	W
Operating Temperature*	T_{opr}	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* under bias

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{EE}	−5.46	−5.2	−4.94	V
Input Voltage	V_{IH}	−1.025	—	—	V
	V_{IL}	—	—	−1.520	V
Operating Temperature	T_{opr}	0	—	75	°C

■ PIN ARRANGEMENT



(Top View)

The V_{BB} reference voltage is available on pin 1 for use in single ended input biasing

■ TRUTH TABLE

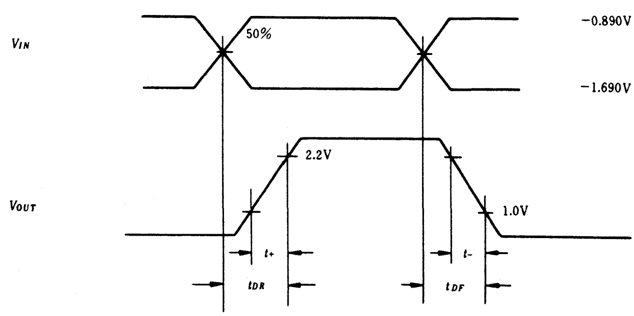
Input		Output
A	B	Y
H	V_{BB}	L
L	V_{BB}	H
H	L	L
L	H	H
V_{BB}	H	H
V_{BB}	L	L
Open	Open	H

■ DC CHARACTERISTICS

Item	Symbol	Test Condition	min	typ	max	Unit
Power Supply Drain Current	$-I_{EE}$	$V_{EE}=-5.2V$, $V_{CC}=5.0V$	—	22	27	mA
	I_{CCH}		—	23.5	29	mA
	I_{CCL}		—	34.5	42	mA
Input Current	I_{inH}	$V_{IN}=-0.81V$	—	—	115	μA
Input Leakage Current	I_{CBO}	$V_{IN}=-5.2V$	—	—	1.0	μA
Output Voltage	V_{OH}	$I_{OH}=-1.0mA$	2.7	—	—	V
	V_{OL}	$I_{OL}=5.0mA$	—	—	0.5	V
Threshold Voltage	V_{OHA}	$V_{IH}=-1.1V$, $I_{OH}=-1.0mA$	2.7	—	—	V
	V_{OLA}	$V_{IL}=-1.48V$, $I_{OL}=5.0mA$	—	—	0.5	V
Indeterminate Input Protection Tests	V_{OHS}	All inputs $=V_{EE}$	2.7	—	—	V
		All inputs = Open	2.7	—	—	
Reference Voltage	V_{BB}		−1.420	—	−1.150	V
Common Mode Rejection Tests	V_{OHC}	$V_{INH}=0.300V$, $V_{INL}=-0.825V$	2.7	—	—	V
		$V_{INH}=-1.890V$, $V_{INL}=-2.890V$	2.7	—	—	
	V_{OLC}	$V_{INH}=0.300V$, $V_{INL}=-0.825V$	—	—	0.5	V
		$V_{INH}=-1.890V$, $V_{INL}=-2.890V$	—	—	0.5	

■ AC CHARACTERISTICS

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{DR}	50% to +2.2V, $C_L=200pF$	—	—	10	ns
	t_{DF}	50% to +1.0V, $C_L=200pF$	—	—	10	ns
Rise Time	t^+	+1.0V to +2.2V, $C_L=200pF$	—	—	5	ns
Fall Time	t^-	+2.2V to +1.0V, $C_L=200pF$	—	—	5	ns



CROSS-REFERENCE

Note)

Type No.	Package Material	Access Time ns (max)
HM4864-2	C	150

1. MOS RAM

Mode	Structure	Total Bit	Organization	Number of Pin	Hitachi	Intel	Texas
Dynamic	NMOS	16k	16384×1	16	HM4716A-1 120 P, G		
					HM4716A-2 150 P, G	2117-2 150 P, G	TMS4116-15 150 P, G, C
					HM4716A-3 200 P, G	2117-3 200 P, G	TMS4116-20 200 P, G, C
					HM4716A-4 250 P, G	2117-4 250 P, G	TMS4116-25 250 P, G, C
					HM4816A-3 100 P, G	2118-3 100 P, G	
					HM4816A-4 120 P, G	2118-4 120 P, G	
					HM4816A-7 150 P, G	2118-7 150 P, G	
		64k	65536×1	16			
					HM4864A-12 120 P, G		
					HM4864-2 150 P, G		TMS4164-15 150 C
					HM4864-3 200 P, G		
Static	NMOS	4k	1024×4	18		2114AL-1 100 P, G	
						2114AL-2 120 P, G	
					HM472114A-1 150 P, G	2114AL-3 150 P, G	
					HM472114A-2 200 P, G	2114A/L-4 200 P, G	
						2114A-5	
					HM472114-3 300 P, G		
					HM472114-4 450 P, G		
					(HM6148) 70 P	2148 70 P, G	
					(HM6148-6) 85 P	2148-6 85 P, G	
			4096×1	18	(HM6147H-35) 35 P, G	2147H-1 35 G, C	
					(HM6147H-45) 45 P, G	2147H-2 45 G, C	
					(HM6147-3) 55 P, G	2147H-3 55 G, C	

Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu	Remarks
					MB8216E 120 C	
MK4116-2 150 P, G	MCM4116-15 150 P, G	µPD416-3 150 P, G	TMM416-2 150 P, G	M5K4116-2 150 P, C	MB8116H 150 C	
MK4116-3 200 P, G	MCM4116-20 200 P, G	µPD416-2 200 P, G	TMM416-3 200 P, G	M5K4116-3 200 P, C	MB8116E 200 C	
MK4116-4 250 P, G	MCM4116-25 250 P, G	µPD416-1 250 P, G	TMM416-4 250 P, G		MB8116N 250 C	
	MCM4116-30 300 P, G	µPD416 300 P, G				
MK4516-10 100 P, G	MCM4516-10 100 P, G				MB8118-10 100	5V single
MK4516-12 120 P, G	MCM4516-12 120 P, G				MB8118-12 120	
MK4164-10 100 P, G						
MK4164-12 120 P, G			TMM4164-2 120 C			
	MCM6664-15 150 C	µPD4164-3 150 C	TMM4164-3 150 C	M5K4164-15 150 C	MB8264-15 150 C	5V single
	MCM6664-20 200 C	µPD4164-2 200 C		M5K4164-20 200 C	MB8264-20 200 C	
	MCM6664-25 250 C	µPD4164-1 250 C				
		µPD2114L-5 150 P, G				
MK4114-3 200 P, C	MCM21/L14-20 200 P, C	µPD2114L-3 200 P, G	TMM314A/L-1 200 P	M5L2114L-2 200 P, C	MB8114E/L 200 P, C	
MK4114-4 250 P, C	MCM21/L14-25 250 P, C	µPD2114L-2 250 P, C				
MK4114-5 300 P, C	MCM21/L14-30 300 P, C	µPD2114L-1 300 P, C	TMM314A/L-3 300 P	M5L2114L-3 300 P, C	MB8114N/L 300 P, C	
	MCM21/L14-45 450 P, C	µPD2114 450 P, C	TMM314A/L 450 P	M5L2114L 450 P, C		
MK2148-70 70 G, C					MB8148-70/L 70 G	
MK2148-85 85 G, C						
					MB8147F-35 35 G	
					MB8147F-45 45 G	
MK4027-55 55 P, G		µPD2147-3 55 G	TMM315-1 55 G		MB8147H 55 G	

Mode	Structure	Total Bit	Organization	Number of Pin	Hitachi			Intel			Texas		
Static	NMOS	4k	4096×1	18	(HM6147/L)	70	P, G	2147/L	70	P, G	2147/L-7	70	P, G
								2147-6	85	P, G	2147-9	90	P, G
		16k	2048×8	24									
					(HM6116/L-2)	120	P						
					(HM6116/L-3)	150	P						
					(HM6116/L-4)	200	P						
											4016-45	450	P
			16384×1	20	(HM6167-3)	55	P	2167-3	55	G			
					(HM6167)	70	P	2167	70	G			
	CMOS	4k	4096×1	18	HM6147/L-3	55	P, G						
					HM6147/L	70	P, G						
					HM4315	450	P						
			1024×4	18	HM6148/L	70	P						
					HM6148/L-6	85	P						
					HM4334-3	300	P, G						
					HM4334-4	450	P, G						
		16k	2048×8	24	HM6116/L-2	120	P, G						

Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu	Remarks
MK4027-70 70 P, G		μPD2147-2 70 G	TMM315 70 G		MB8147E 70 G	
MK4027-90 90 P, G					MB8147N 95 G	
MK4802-70 70 G, C						
MK4802-90 90 G, C						
MK4802-1 120 P, G, C		(μPD446-2) 120 P, G	TMM2016-1 100 P		MB8128-10 100	
		(μPD446-1) 150 P, G	TMM2016 150 P	M58725-15 150 P, G	MB8128-15 150	
MK4802-3 200 P, G, C		(μPD446) 200 P, G		M58725 200 P, G		
					MB8167-55 55 G	
					MB8167-70 70 G	
					MB8404E 250 G	
	MCM16504 450 P		TC5504 450 P			HM6504 Compati.
			TC5504-1 550 P			
			TC5504-2 800 P			
		μPD444-3 200 P				
		μPD444-2 250 P			MB8414E 250 G	
		μPD444-1 300 P				HM6514 Compati.
		μPD444 450 P	TC5514 450 P	M58981-45 450 P, C		
			TC5514-1 650 P			
			TC5514-2 800 P			
		μPD446-2 120 P				} Hitachi Pin

Mode	Structure	Total Bit	Organization	Number of Pin	Hitachi	Intel	Texas
Static	CMOS	16k	2048×8	24	HM6116/L-3 150 P, G		
					HM6116/L-4 200 P, G		
					HM6117/L-3 150 P		
					HM6117/L-4 200 P		

2. MOS ROM

Program	Structure	Total Bit	Organization	Number of Pin	Hitachi	Intel	Texas
Mask	NMOS	32k	4096×8	24	HN46332 350 P		TMS4732 450 P, G
						2332A 450 P, G	
		64k	8192×8	24			
					HN48364 350 P		TMS4764 350 P
				28		2364A 450 P, G	
Electrically & UV Erasable	NMOS	16k	2048×8	24	HN462716-1 350 G	2716-1 350 G, C	
					HN462716-2 390 G	2716-2 390 G, C	
					HN462716 450 G, C	2716 450 G, C	TMS2516 450 G, C
						2716-5 490 G, C	
						2716-6 650 G, C	
		32k	4096×8	24	HN482732A-20 200 G	2732A-2 200 G, C	
					HN482732A-25 250 G	2732A 250 G, C	
					HN482732A-30 300 G	2732A-3 300 G, C	
					HN462732-2 390 G, C	2732 450 G, C	
					HN462732 450 G, C	2732-6 550 G, C	
					HN462532-2 390 G		TMS2532-25 250 G, C

Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu	Remarks
		μPD446-1 150 P				Hitachi Pin
		μPD446 200 P			MB8416 200	
		μPD447-2 120 P				Toshiba Pin
		μPD447-1 150 P				
		μPD447 200 P	TC5516A 250 P		MB8417 200	
						NEC Pin
		μPD449 200 P			MB8418 200	

Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu	Remarks
MK32000-5 300 P, G	MCM68A332 350 P, C	μPD2332 450 P, G	TMM333 450 P	M58333 650 P	MB8332 200 P	Texas Pin
			TMM2332 350 P		MB8333 200 P	Intel Pin
MK36000-4 250 P, G, C	MCM68B364 250 P, C				MB8364 250 P	
MK36000-5 300 P, G, C	MCM68A364 350 P, C	μPD2364 450 P, G		M58334 650 P		
MK37000-4 250 P, G			TMM2364 250 P			
MK2716-6 350 G	MCM27A16 350 C				MB8516H 350 G, C	
MK2716-7 400 G						
MK2716-8 450 G	MCM2716 450 C	μPD2716 450 G, C	TMM323 450 G, C	M5L2716 450 G	MB8516 450 G, C	
MK2716-12 650 G						
					MBM2732A-20 200	Intel Pin
					MBM2732A-25 250	
					MB8532-35 350 C	
		μPD2732 450 G	TMM2732 450 G	M5L2732 450 G	MB8532-45 450 C	
				M5L2732-6 550 G		
	MCM25A32 350 C					Texas Pin

Program	Structure	Total Bit	Organization	Number of Pin	Hitachi		Intel		Texas	
Electrically & UV Erasable	NMOS	32k	4096×8	24	HN462532				TMS2532-45	
					450	G, C			450	G, C
		64k	8192×8	28			2764-2			
							200	G		
					HN482764		2764			
					250	G, C	250	G		
					HN482764-3		2764-3		TMS2564-35	
					300	G, C	300	G	350	G, C
					HN482764-4				TMS2564-45	
					450	G, C			450	G, C
Electrically Erasable	NMOS	16k	2048×8	24	HN48016		2816			
					350	P	250			
							2816-3			
							350			

3. BIPOLAR RAM

Structure	Total Bit	Organization	Number of Pin	Output	Hitachi		Fairchild		Texas	
TTL	256	256×1	16	O/C	HM2504-1		93411A			
					45	G	45	G		
					HM2504		93411		SN74S301	
					55	G	55	G, F	42	P, G
	1k	1024×1	16	O/C	HM2510-2		93415A			
					35	G	30	G, F		
					HM2510-1		93415			
					45	G	45	P, G, F		
					HM2510				SN74S314A	
					70	G			70	P, G
				3-S			93425A			
							30	G, F		
					HM2511-1		93425			
					45	G	45	G, F		
					HM2511				SN74S214A	
					70	G			70	P, G
ECL	256	256×1	16		HM2105		F10410		SN10144	
					35	G	30	P, G, F	30	G, F
					HM10414-1					
					8	G				
					HM10414		F10414			
					10	G	10	G		
					HM2106		F10411			
					15	G	35	P, G, F		
	1k	256×4	24		HM10422		F10422			
					10	G	10	G, F		
					HM100422		F100422			
					10	G, F	10	G, F		
		1024×1	16		HM2110-2		F10415A			
					20	G	20	G, F		
					HM2110-1					
					25	G				
					HM2110		F10415			
					35	G	35	G, F		

Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu	Remarks
	MCM2532 450 | G, C					Texas Pin
	MCM68764 450 | C (24Pin)				MBM2764-20 200 |	Intel Pin
MK2764-8 450 | C					MBM2764-25 250 |	
					MBM2764-30 300 |	Texas Pin
						2816 : Byte Erase 10ms

Intel	Motorola	MMI	Signetics	NEC	Fujitsu	Remarks
3107A 60 | G, C			N82S117 40 | G			
3107 80 | G, C		6530 55 | C	74S301 50 | G	μPB2206 50 | G		
			N93415A 35 | G			
	MCM93415 45 | P, G, F		N93415 45 | G	μPB2205 50 | G	MBM93415 45 | G	
			N93425A 35 | G			
	MCM93425 45 | G, F		N93425 45 | G			
	MCM10144 30 | G, F			μPB10144 25 | G	MB7044 35 | G	
					MB7042H 12 | G	
	MCM10152 45 | G, F				MB7042 15 | G	
					MB7074 10 | G	
					MB7046H 20 | G	
	MCM10146 30 | G, F				MB7046 35 | G	

Structure	Total Bit	Organization	Number of Pin	Output	Hitachi	Fairchild	Texas
ECL	1k	1024×1	16		HM100415 35 G	F100415 35 G, F	
	4k	1024×4	18		HM10474 25 G	F10474 30 G, F	
					HM100474 25 G, F	F100474 30 G, F	
		4096×1	18		HM10470-1 15 G		
					HM10470 25 G	F10470 35 G, F	
					HM100470 25 G	F100470 35 G, F	

3. BIPOLAR PROM

Structure	Total Bit	Organization	Number of Pin	Output	Hitachi	Fairchild	Texas
TTL	4k	1024×4	18	O/C			
							TBP24SA41 40 P, G
					HN25044 50 G	93452 55 G	
				3-S			
							TBP24S41 40 P, G
					HN25045 50 G	93453 55 G	
	8k	2048×4	18	O/C	HN25084 60 G		TBP24SA81 45typ P, G
				3-S	HN25085 60 G		TBP24S81 45typ P, G
		1024×8	24	O/C	HN25088 60 G	93450 55 G, F	TBP28SA86 60 P, G
				3-S			
					HN25089 60 G	93451 55 G, F	TBP28S86 60 P, G
	16k	2048×8	24	O/C	HN25168 60 G	93510 55 G, F	
				3-S	HN25169 60 G	93511 55 G, F	TBP28S166 45typ G

Intel	Motorola	MMI	Signetics	NEC	Fujitsu	Remarks
					MB7076 25 C	
					MB7078 35 C	

Intel	Motorola	MMI	Signetics	NEC	Fujitsu	Remarks
					MB7121H 35 G	
					MB7121E 45 G	
3605A-1 50 G						
3605A-2 60 G	MCM7642 70 G	6352-1 60 G	N82S136 60 G	μPB406 70 G	MB7059 70 G	
					MB7122H 35 G	
					MB7122E 45 G	
3625A-1 50 G						
3625A-2 60 G	MCM7643 70 G	6353-1 60 G	N83S137 60 G	μPB426 70 G	MB7054 70 G	
	MCM7684 80 G		N82S184 100 C			
	MCM7685 80 G		N82S188 100 C		MB7128E 55 G	
3608 80 G	MCM7680 70 G	6380-1 90 G	N82S182 60 G	μPB408 85 G	MB7060 250 G	
3628A-1 50 G						
3628A 60 G	MCM7681 70 G	6381-1 90 G	N82S183 60 P, G	μPB428 85 G	MB7132E 55 G	
3628 80 G						
3628-4 100 G					MB7055 250 G	
			N82S190 80 C			
3636-1 65 G			N82S191 80 C		MB7138E 55 G	
3636 80 G						

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